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REMOVABLE CARTRIDGE DISK DRIVE WITH ANGULARLY INSERTED CARTRIDGES ;

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ABSTRACT:

A removable cartridge disk drive (100) that receives cartridges at an angle relative to the base of the drive. The removable cartridge disk drive ejects cartridges (101) at an angle relative to the base of the drive such that the cartridge opens the disk drive door (286). The removable cartridge may contain multiple disks and is further configured to conform to a 3.5 inch form factor while the corresponding disk drive has a drive height of 1 inch or less. The removable cartridge disk drive also has a bent wire (246) mounted to a suspension on the actuator (110) that engages a head load/unload ramp while a head is over the disk, thereby permitting the disk drive to utilize a stationary head load/unload ramp. The disk drive further has a Burst In Range mode that ignores servo errors unless the servo error occurred during a target data sector and unless the servo error is a certain type of servo error. A history of recent error conditions is maintained. The Special Data Sector mode identifies the exact data sector during which a servo error was detected. The removable cartridge used by the disk drive has an anti-rattle feature.

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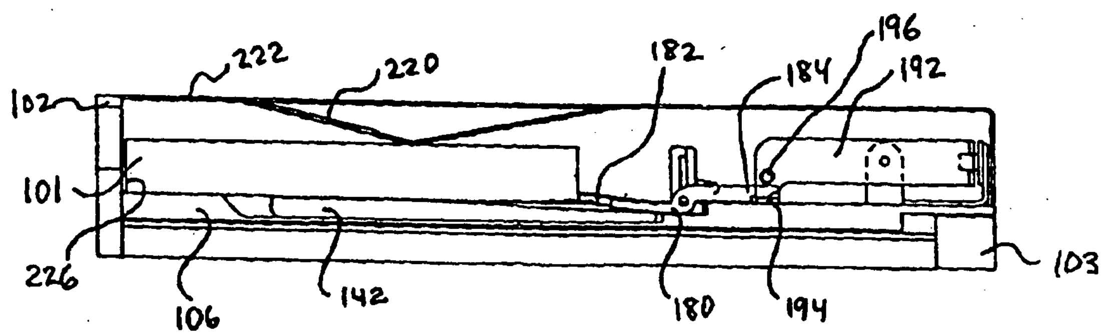

(57) Abstract

A removable cartridge disk drive (100) that receives cartridges at an angle relative to the base of the drive. The removable cartridge disk drive ejects cartridges (101) at an angle relative to the base of the drive such that the cartridge opens the disk drive door (286). The removable cartridge may contain multiple disks and is further configured to conform to a 3.5 inch form factor while the corresponding disk drive has a drive height of 1 inch or less. The removable cartridge disk drive also has a bent wire (246) mounted to a suspension on the actuator (110) that engages a head load/unload ramp while a head is over the disk, thereby permitting the disk drive to utilize a stationary head load/unload ramp. The disk drive further has a Burst In Range mode that ignores servo errors unless the servo error occurred during a target data sector and unless the servo error is a certain type of servo error. A history of recent error conditions is maintained. The Special Data Sector mode identifies the exact data sector during which a servo error was detected. The removable cartridge used by the disk drive has an anti-rattle feature.

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DESCRIPTION

REMOVABLE CARTRIDGE DISK DRIVE WITH ANGULARLY INSERTED CARTRIDGES

Cross Reference To Related Applications

This non-provisional patent application claims the benefit of U.S. Provisional Application Serial No. 60/006,635, which was filed on November 13, 1995.

Field of the Invention

The field of the present invention is removable cartridge disk drives.

Background of the Invention

There is a growing demand for powerful yet inexpensive portable computers capable of high memory capacity. A known method of achieving high memory capacity is to employ a removable cartridge disk drive. In such a disk drive, any number of removable cartridges can be used to store as much data as is required for use with the computer. Additionally, this data can be secured in a safe location remote from the computer in order to ensure the confidentiality of the data when the computer is not in use. To minimize the cost of such a disk drive, speed and efficiency of manufacture are essential. Thus, it is desirable to construct the disk drive so that it uses as few moving parts as possible in receiving an inserted cartridge.

Traditionally, removable cartridge disk drives have been constructed such that after the cartridge is inserted the drive engages it in one of two ways: Either (1) the cartridge is received and subsequently lowered onto the spindle motor of the drive; or (2) the cartridge is received and then the spindle motor moves upward to engage

it. Such designs have generally proven effective in keeping down the number of moving parts used and allowing the removable cartridge and disk drive to be as compact as possible. However, in light of the ever increasing demand for lower costs in conjunction with higher data storage capacity, it is necessary to further reduce the number of components used.

It is known in the art to construct a disk drive that uses a rotary actuator arm which accesses the removable cartridge and carries read/write transducer heads over the surface of the disk contained in the cartridge. Traditionally, the heads have been loaded onto the disk. or unloaded off of it, by means of a movable ramp. Although use of a fixed ramp is desirable from a manufacturing standpoint, it has proven necessary to use a movable ramp for the following reasons. If the ramp were fixed, it would either have to be made extremely thin so as to fit between the head and the surface of the disk, which would render the ramp too fragile, or have to be constructed with a forked end to encompass the perimeter of the disk, which would add to manufacturing cost.

For the foregoing reasons, there is a need for a disk drive that minimizes the number of parts utilized in receiving, holding, accessing, and ejecting a removable cartridge; allows a fixed ramp to be used for loading and unloading the read/write transducer heads; and frees the actuator arm to rotate far enough to place the heads outside the cartridge and beyond the perimeter of the disk.

Summary of the Invention

The present invention is directed to a removable cartridge disk drive and a removable cartridge disk drive system.

A first, separate aspect of the present invention is a removable cartridge disk drive that receives cartridges at an angle relative to the base of the drive.

A second, separate aspect of the present invention is a removable cartridge disk drive that ejects cartridges at an angle relative to the base of the drive such that the cartridge opens the disk drive door.

A third, separate aspect of the present invention is a removable cartridge multi-platter disk drive that receives cartridges at an angle relative to the base of the drive and is configured to conform to a 3.5 inch form factor while maintaining a drive height of 1 inch or less.

A fourth, separate aspect of the present invention is a removable cartridge disk drive that has a bent wire mounted to a suspension on the actuator such that the bent wire engages a head load/unload ramp while a head is over the disk.

A fifth, separate aspect of the present invention is a removable cartridge disk drive that has a stationary head load/unload ramp which does not protrude into an opening of the cartridge.

Another separate aspect of the present invention is a disk drive having circuitry that ignores servo errors unless the servo error occurred during a data sector which is to be read from or written to and unless the servo error is a certain type of servo error.

Yet another separate aspect of the present invention is a disk drive having a servo burst in range mode that identifies the data sector during which a servo error was detected.

Still another separate aspect of the present invention is a removable cartridge having an anti-rattle feature that is deactivated when the cartridge door is opened.

Additional advantages and separate aspects of the present invention will be set forth in the description that follows and in part will be obvious from that description or can be learned by practicing the invention.

Brief Description of the Drawings

The various aspects, features and advantages of the present invention will be better understood by examining the Detailed Description found below, together with the attached Drawings, wherein:

FIG. 1 shows a top interior plan view of an embodiment of a disk drive and removable cartridge incorporating aspects of the present invention, with the actuator in the unloaded position.

FIG. 2 shows a top interior plan view of an embodiment of a disk drive and removable cartridge incorporating aspects of the present invention, with the actuator in the loaded position.

FIG. 3 shows a front plan view of the disk drive door.

FIG. 4 shows a top down view of the drive door.

FIG. 5 shows an end view of the drive door.

FIG. 6 shows a top plan view of the slide used in the insertion and ejection of a removable cartridge from an embodiment of a disk drive incorporating aspects of the present invention.

FIG. 7 shows a left side view of the slide used in the insertion and ejection of a removable cartridge from an embodiment of a disk drive incorporating aspects of the present invention.

FIG. 8 shows a right side view of the slide used in the insertion and ejection of a removable cartridge from an embodiment of a disk drive incorporating aspects of the present invention.

FIG. 9 shows a back end view of the slide used in the insertion and ejection of a removable cartridge from an embodiment of a disk drive incorporating aspects of the present invention.

FIG. 10 shows a top plan view of the grooves formed in the drive base to define the traveling motion of the slide, slide arms, catch and slide spring.

FIGs. 11A-11F are right side plan views showing the progression of parts in a disk drive embodying aspects of the present invention as a cartridge is initially inserted into the disk drive (FIG. 11A) and moved to its fully inserted position (FIG. 11E).

FIG. 12 shows a top plan view of a catch.

FIG. 13 shows a side edge view of the catch in FIG. 12.

FIG. 14 shows a top plan view of a release link.

FIG. 15 shows a side edge view of the release link as taken along line A-A in FIG. 14.

FIG. 16 shows an end view of the release link in FIG. 14.

FIG. 17 shows a top view of a solenoid link.

FIG. 18 shows a side view of the solenoid link in FIG. 17.

FIG. 19 shows a see-through view of the back end of a disk drive embodying aspects of the present invention when the cartridge is in its fully inserted position.

FIG. 20 shows a see-through view of the back end of a disk drive embodying aspects of the present invention when the cartridge is being ejected out of the disk drive.

FIG. 21 shows a top plan view of a retract lever used to retain the actuator in an unloaded position.

FIG. 22 shows a side view of a retract lever used to retain the actuator in an unloaded position.

FIG. 23 shows a top view of an actuator with a bent wire for an embodiment of a disk drive incorporating aspects of the present invention.

FIG. 24 shows a perspective view of an actuator with bent wires for an embodiment of a two-disk disk drive incorporating aspects of the present invention.

FIG. 25 shows a side view of an actuator with bent wires for an embodiment of a two-disk disk drive incorporating aspects of the present invention.

FIG. 26 shows a top plan view of a fixed ramp used to load and unload read/write heads in an embodiment of the present invention.

FIG. 27 is a side view of the head load/unload ramp of FIG. 26 as taken along the line marked A-A in FIG. 26.

FIG. 28 is a view of the head load/unload ramp of FIG. 27 as taken along the line marked B-B in FIG. 27.

FIG. 29 shows a top plan view of the actuator with its read/write heads loaded onto a disk in a removable cartridge.

FIG. 30 shows a top plan view of the actuator with its read/write heads parked on the head load/unload ramp.

FIG. 31 shows a closeup cross-sectional side view of the actuator of FIG. 30 in its unloaded position.

FIG. 32 shows a closeup cross-sectional side view of the actuator of FIG. 29 in its loaded position.

FIG. 33 shows a top plan view of a retaining wire used to restrain a propelled slide incorporating aspects of the present invention.

FIGs. 34A-34F are right side plan views showing the progression of parts in an embodiment of a disk drive incorporating aspects of the present invention as the process of ejecting a removable cartridge starts (FIG. 34A) and finishes (FIG. 34F).

FIG. 35 shows a top interior plan view of a removable cartridge with the cartridge door in a closed position.

FIG. 36 shows a top interior plan view of a removable cartridge with the cartridge door in a partially opened position.

FIG. 37 shows a top interior plan view of a removable cartridge with the cartridge door in a completely opened position.

FIG. 38 shows a top plan view of a cartridge plunger used in the anti-rattle feature of the removable cartridge.

FIG. 39 shows a side view of the cartridge plunger of FIG. 38.

FIG. 40 is a cross-sectional side view of the cartridge plunger as taken across the section A-A marked in FIG. 38.

FIG. 41 shows a perspective view of a cartridge hub used in the anti-rattle feature of the removable cartridge.

FIG. 42 is a side view of the cartridge hub used in the anti-rattle feature of the removable cartridge shown in FIG. 41.

FIG. 43 is a cross-sectional side view of the cartridge hub used in the anti-rattle feature of the removable cartridge shown in FIG. 41.

FIG. 44 is a top plan view showing the interaction between the cartridge hub of FIG. 41 and the cartridge plunger of FIG. 38 as used in the anti-rattle feature of a removable cartridge.

FIG. 45 is a see-through cross-sectional side view of the removable cartridge and depicts the interaction between the cartridge plunger, cartridge hub and the rest of the cartridge when the anti-rattle mode is activated.

FIG. 46 is a simplified block diagram of circuitry that conceptually illustrates a servo error register, mask circuit and drive interface status register as used in an embodiment of a disk drive with a servo burst in range mode.

FIG. 47 is a detailed block diagram of circuitry that illustrates a servo error register, mask circuit and drive interface status register as used in an embodiment of a disk drive with a servo burst in range mode.

FIG. 48 illustrates a representation of a portion of a track on the disk having servo sectors that comprise servo fields and data sectors as well as a timing diagram with four waveforms depicting the behavior of an embodiment of a disk drive that maintains a history of error conditions.

FIG. 49 is a timing diagram showing the states of various signals and registers during the cycle of

initializing a Burst In Range mode, entering the Burst In Range mode, and detecting error conditions during the Burst In Range mode in a disk drive embodying the present invention.

FIG. 50 illustrates a representation of a portion of a track on the disk and a timing diagram depicting the operation of the Special Data Sector mode. The timing diagram has four waveforms showing servo synchronization mark pulses, sector mark pulses, the contents of the Last Data Sector Number register (LDSEC register) and the contents of the Burst Data Sector Number register (BDSEC register).

FIG. 51 is a top level diagram of major constituent components in the ASIC used to implement a Burst In Range mode and a Special Data Sector mode in a disk drive.

FIG. 52 is a detailed circuit diagram of circuitry contained within the SECTPEQ2 block of FIG. 51.

FIG. 53 is a detailed circuit diagram of circuitry contained in the SECTOR2 block of FIG. 52.

FIG. 54 is a detailed circuit diagram of circuitry contained in the Burst In Range (BRSTRNG) circuit block of FIG. 53.

FIG. 55 is a detailed circuit diagram of circuitry contained in the K21INT block of FIG. 51.

FIG. 56 is a detailed circuit diagram of circuitry contained in the INTERPT block of FIG. 55 which implements a servo error status register, drive interface status register and associated logic circuitry.

FIG. 57 is a detailed circuit diagram of circuitry contained in the INTERPT block of FIG. 55 which implements a mask count register.

FIG. 58 is a detailed circuit diagram of circuitry contained in the INTERPT block of FIG. 55 which implements mask counters.

FIG. 59 is a detailed circuit diagram of circuitry contained in the INTERPT block of FIG. 55 which implements a Last Data Sector Number (LDSEC) register.

FIG. 60 is a detailed circuit diagram of circuitry contained in the INTERPT block of FIG. 55 which implements a Burst Data Sector Number (BDSEC) register.

FIGs. 61-63 are detailed circuit diagrams of the three-bit and two-bit counters which are used to implement mask counters in FIG. 58.

FIGs. 64A-64B are software flowcharts for implementing a Burst In Range mode and a Special Data Sector mode in a disk drive embodying the present invention.

Detailed Description of the Preferred Embodiment

FIG. 1 illustrates an internal top plan view of a preferred embodiment of a removable cartridge disk drive utilizing aspects of the present invention. The disk drive 100, shown with a removable cartridge 101 fully inserted therein, has an outer housing comprising a drive front end 102, drive back end 103, left side wall 104 and right side wall 105, all of which are mounted to a drive base 106 and support a top plate (not shown). The top plate is not shown in order to highlight the internal mechanisms of the disk drive 100. In a preferred embodiment, the drive front end 102, drive back end 103, left side wall 104, right side wall 105 and drive base 106 are manufactured of a metal such as aluminum, which may be extruded, casted or formed. Mounted to the drive base 106 is a spindle motor 107 (under the disk 108 and cartridge 101) that serves to rotate at least one disk 108 contained in the cartridge 101. In a preferred embodiment, the cartridge 101 has two disk platters 108. Also mounted to the drive base 106 is a voice coil motor 109 that controls the angular rotation of a rotary actuator 110. The planar surfaces of the disk 108 may contain one or more calibration tracks with alternating servo burst patterns for removing offset caused by magnetic distortion as disclosed in U.S. Patent No. 5,400,201 assigned to the

assignee of the present invention and fully incorporated herein by reference.

FIG. 3 is a front plan view of the disk drive door 120 that is mounted by hinges 122 at the bottom corners of the drive door 120 to the drive front end 102. FIG. 4 depicts a top down view of the drive door 120 and FIG. 5 shows an end view of the drive door 120. The disk drive door 120 covers a cartridge receiver opening 124 through which the disk drive 100 receives the cartridge 101. The drive door 120 further includes a handle 126 for a user to manually open the drive door 120, a stop bar 128 for controlling the extent of the drive door 120 opening motion, a recess 130 for placement of a label and an LED opening 134 for LEDs that indicate the status of the disk drive 100. Integrally formed and extending from the back surface of the drive door 120 are two rub rails 132. As will be explained, an ejecting cartridge impacts these two rub rails 132 to open the drive door 120 and protrude sufficiently from the cartridge receiver opening 124 so that a user can manually grasp and remove the ejected cartridge.

The insertion and ejection of the cartridge 101 into and from the disk drive 100 are described next. FIG. 1 illustrates an internal top plan view of a preferred embodiment of a disk drive 100 and a removable cartridge 101 with a disk 108 incorporating aspects of the present invention. FIG. 2 depicts the disk drive 100 and removable cartridge 101 with the read/write transducer heads 140 loaded onto the disk 108. As is apparent in FIG. 1, the disk drive 100 includes a slide 142 located between the spindle motor 107 and the right side wall 105. The slide 142 is preferably manufactured as a unitary structure and made of a relatively slick plastic having a low friction coefficient such as delrin.

The slide 142 is shown in greater detail in FIGs. 6-9. FIGs. 6-9 illustrate a top plan view, a left side view, a right side view and a back end view of the slide

142. The slide 142 has a body 144, a cam nose end 145 and a pair of slide arms 146, 148. The slide arm 148 located closest to the right side wall 105 has a tab 150 uprising from one end of the slide arm 148. The tab 150 has a protrusion 152 extending outwardly towards the right side wall 105. The right slide arm 148 further has a hole 153 for receiving a pivot pin 155. The pivot pin 155 can be seen in FIG. 11A.

The slide 142 rides in a groove 154 formed in the drive base 106. This groove 154 is illustrated in FIG. 10 and comprises several groove portions: slide groove 156, arm grooves 158, spring groove 160 and catch groove 162. Arm grooves 158 slope downward relative to the surface of the drive base 106, where the deepest portions of the arm grooves 158 are located nearest the drive back end 103 and the shallowest portions of the arm grooves 158 are located nearest the drive front end 102. Thus, as the slide 142 and its slide arms 146, 148 travel in their respective grooves toward the drive back end 103, the slide 142 moves at a downward angle relative to the drive base 106 until the top surface of the slide 142 is flush with the top surface of the drive base 106.

Referring to FIG. 1, a slide spring 164 rests in the spring groove 160 and has a first end 168 that is connected to a pin 170 on the body of the slide 142 and a second end 172 that is connected to a drive base post 174 uprising from and integrally formed with the drive base 106. The slide spring 164 biases the slide 142 to ride in the groove 154 toward the drive front end 102.

The right slide arm 148 further has a cavity 176, shown in FIG. 6, that holds one end of a catch spring 178. The second end of the catch spring 178 attaches to a catch 180, as illustrated in the plan views of the right side of the disk drive 100 in FIGs. 11A-11E.

The catch 180 has a first end 182, a second end 184, a stop member 186 and a pivot hole 188, as shown in the top plan view of the catch in FIG. 12. A pin 155 threads

through the pivot hole 188 of the catch 180 and the pivot hole 153 of the slide 142 to cause the catch 180 to be pivotally mounted to the slide 142. The first end 182 of the catch 180 is for contacting by the forward end 190 of the cartridge 101 while the second end 184 of the catch 180 is for engaging a release link 192.

The release link 192 pivots about pin 155 that is mounted to the right side wall 105 of the disk drive 100. FIGs. 14-16 depict the release link 192 in a top plan view, a side edge view and an end view respectively. FIG. 15 is a view taken along the line A-A of FIG. 14. As illustrated, the release link 192 has a lift plate 194, a safety post 196 and a tail end 198. Returning to FIGs. 1 and 11A-11E, the tail end 198 of the release link 192 is pivotally attached by a pivot pin 199 to a solenoid link 200 which in turn is pivotally connected to the plunger 202 of the solenoid 204. The pivot pin 199 attaches the tail end 198 of the release link 192 to the solenoid link 200 by the first pivot hole 206 of the solenoid link 200, as shown in the top and side views of the solenoid link 200 in FIGs. 17 and 18.

FIGs. 19 and 20 show various drive components as seen through the drive back end 103. The solenoid link 200 has a cam surface 208 that engages a camming pin 210 located on the plunger 202. The solenoid link 200 has a second pivot hole 212 that engages a pivot pin 214 mounted to the drive back end 103, thereby allowing the solenoid link 200 to pivot between two positions. A spring 216 has one end attached to a spring post 218 formed on the solenoid link 200 and the other end connected to the drive base 106, thereby biasing the solenoid link 200 to its rest position, shown in FIGs. 19 and 20 as a horizontal position. Although the rest position of the solenoid link 200 is shown to be a horizontal position, the rest position may be any position.

The operation of these disk drive components during insertion of a cartridge 101 into the disk drive 100 is as

follows. FIGs. 11A-11E are right side plan views showing the progression of parts in the disk drive 100 as a cartridge 101 is initially inserted into the disk drive 100 (FIG. 11A) and moved to its fully inserted position (FIG. 11E).

Referring to FIG. 11A, a cartridge 101 has been partially inserted into the disk drive 100. A pair of bias springs 220 (one of which is illustrated) is mounted to and extends downwardly from the bottom surface of the disk drive top cover 222. The pair of bias springs 220 applies pressure to the top surface of the cartridge 101 and guides the cartridge 101 such that the cartridge 101 inserts at a angle relative to the drive base 106. In FIG. 11A, the cartridge 101 has been inserted into the disk drive 100 such that the forward end 190 of the cartridge 100 rests on the slide 142 and has just contacted but not moved the first end 182 of the catch 180. The forward end 190 of the cartridge 101 does not contact the tab 150 of the slide 142 because the first end 182 of the catch 180 keeps the forward end 190 of the cartridge 101 from contacting the tab 150. The corner of the cartridge's forward end 190 is kept away from the tab 150 by a distance approximately equal to the length of the first end 182 of the catch 180.

At this stage, the catch 180 is biased by the catch spring 178 to its initial and rest position. When the catch 180 is in this rest position, the stop member 186 of the catch 180 is pressed against the protrusion 152 that extends outwardly from the tab 150 of the slide 142. Further, the first end 182 of the catch 180 is in a position that is ready to engage the forward end 190 of the cartridge 101. Although this ready position of the first end 182 of the catch 180 is shown to be angled upward toward the drive front end 102, the ready position may be any position that contacts a portion of the cartridge 101. The second end 184 of the catch 180 does not contact the release link 192 yet.

The slide 142 is also in its rest position since the slide spring 164 that biases the slide 142 to this rest position is in a relaxed state. That is, the end of the slide 142 closest to the drive front end 102 rests on top of the drive base 106 and out of the groove 156.

Referring now to FIGs. 19 and 20, the solenoid 204 can be in one of two states: an electronically picked state and a non-picked state. The solenoid 204 is picked when the user ejects a cartridge. When the solenoid 204 is picked, the plunger 202 moves from its extended position out of the solenoid 204, shown in FIG. 19, to its retracted position, shown in FIG. 20. During the entire cartridge insertion process, the solenoid 204 is in a non-picked state because there is no cartridge to eject. Thus, during the entire process of inserting a cartridge 101 into the disk drive 100, the solenoid link 200 is in its rest position as biased by spring 216 and the plunger 202 is extended out of solenoid 204.

After the cartridge 101 has progressed to the state of partial insertion illustrated in FIG. 11B, the forward end 190 of the cartridge 101 has contacted the first end 182 of the catch 180 and has pushed the catch 180 toward the drive back end 103 but not to the point where the second end 184 of the catch 180 contacts the release link 192. Because the catch 180 is pivotally mounted to the slide 142, the slide 142 is also moved toward the drive back end 103. As the slide 142 travels toward the drive back end 103, the slide spring 164 attached to the slide 142 is increasingly stretched. Additionally, more of the slide 142 now lies in the groove 154 in the drive base 106, but the cam nose end 145 of the slide 142 still resides out of the groove 156.

In FIG. 11C, the cartridge 101 has been inserted to the point where the cam nose end 145 of the slide 142 is about to glide down a cam surface 224 which is depicted as a ramp. The cam surface 224 is preferably made of a slick plastic with a low friction coefficient such as delrin.

The cam surface 224 is mounted inside the groove 156 and at the end of the groove 156 closest to the drive front end 102.

Turning to FIG. 11D, the cartridge 101 has been inserted far enough into the disk drive 100 as to cause the cam nose end 145 of the slide 142 to glide down the cam surface 224 and to lie entirely in the groove 156. The top surface of the slide 142 is now flush with the surface of the drive base 106.

Referring to FIG. 11E, the cartridge 101 is in its fully inserted and locked position within the disk drive 100. The cartridge back end 226 of the cartridge 101 has dropped into the disk drive 100 and the cartridge 101 rests completely within the confines of the disk drive 100. The cartridge 101 rests on the slide 142 parallel to the surface of the drive base 106 such that the disk hub of the cartridge 101 properly engages the spindle motor 107 (which is visible in FIG. 11D). The cartridge 101 has now pushed the catch 180 and the slide 142 even closer towards the drive back end 103. The second end 184 of the catch 180 has now engaged the release link 192 and rests between the lift plate 194 and the safety post 196 of the release link 192. The safety post 196 prevents the catch 180 from inadvertently pivoting counterclockwise due to shock or other trauma to the disk drive 101. Such an undesired pivoting of the catch 180 may cause the accidental ejection of the cartridge 101, as will be described later.

The cartridge 101 is locked in this fully inserted position by the interaction of the catch 180 and the drive front end 102 on the cartridge 101. As previously described, the slide 142 and the catch 180 are urged by the slide spring 164 toward the drive front end 102. However, the slide 142 and the catch 180 cannot move toward the drive front end 102 because the cartridge 101 is sandwiched between the first end 182 of the catch 180 and the drive front end 102. Furthermore, the pair of

bias springs 220 extending from the bottom surface of the drive top cover 222 keeps the cartridge 101 resting on the drive base 106.

FIGs. 21 and 22 illustrate a top plan view and a side view respectively of a retract lever 228. The retract lever 228 has a leg 230, a screw hole 232 and a post 234. Turning to FIG. 1, a screw 236 mounts the retract lever 228 through its screw hole 232 to the top plate of the voice coil motor 109. A spring 238 has one end attached to the retract lever 228 and the other end connected to the post 234. The spring 238 biases the retract lever 228 to rotate clockwise so that the leg 230 of the retract lever 228 presses a retract pin 240 that is upstanding from the actuator 110, thereby forcing the actuator 110 to its unloaded position.

When the cartridge 101 is fully inserted (see e.g., FIG. 2), the tab 150 of the slide 142 engages the post 234 on the retract lever 228, which causes the retract lever 228 to rotate counterclockwise. The counterclockwise rotation of the retract lever 228 causes the leg 230 of the retract lever 228 to release the retract pin 240 on the actuator 110. The heads 140 on the end of the actuator 110 are now free to be rotated by the voice coil motor 109 into the opening of the cartridge 101 and onto the disk 108.

Rotary actuator 110 and its components are more elaborately described in FIGs. 23-25. FIGs. 23-25 are a top plan view, a perspective view and a side view respectively of the actuator 110. As illustrated in FIG. 23, the actuator 110 has a coil 242, a suspension 244, a bent wire 246 and a slider with a read/write transducer head 140. The bent wire 246 has a leg 248 with a foot 250. The leg 248 of the bent wire 246 is affixed to the suspension 244. In a preferred embodiment, the foot 250 of the bent wire 246 angles away from the leg 248 at a 150 degree angle. The heads 140 on the actuator 110 transmit and receive signals from the flexible circuit 252.

In an embodiment of a disk drive that utilizes a two-disk stack, the actuator 110 has three actuator arms 254, 256 and 258. Actuator arms 254 and 258 have one suspension 244 each, while the middle actuator arm 256 has two suspensions 244. Each suspension 244 has a slider with a read/write head 140 mounted thereto. Thus, the actuator 110 is shown with a total of four heads, one for each surface of the two disks.

Since there are four heads, the head load/unload ramp must have multiple ramp surfaces, one to load/unload each head. A ramp 260 with four ramp surfaces 262 is described next. FIG. 26 illustrates a top plan view of a fixed ramp 260 that is mounted to the drive base 106 by two screws. The ramp 260 has a blade segment 264, a rest segment 266 and a ramp surface 262 which has a tip 268. FIG. 27 is a side view of the ramp 260 as taken along the line marked A-A in FIG. 26. FIG. 28 is a view of the ramp 260 taken along the line marked B-B in FIG. 27. Both FIGs. 27 and 28 illustrate the four ramp surfaces 262 for loading and unloading the heads.

The operation of the head unloading process is now described. FIG. 29 shows a top plan view of the actuator 110 with its heads 140 loaded onto the disk 108. When unloading the heads 140 from a disk 108, the voice coil motor 109 (not shown in FIG. 29) rotates the actuator 110 clockwise, causing the foot 250 of the bent wire 246 to contact the ramp surface 262 of the ramp 260. It is noteworthy that although the heads 140 are still loaded onto the disk 108, the foot 250 of the bent wire 246 has already slid onto the ramp surface 262 of the ramp 260, thereby starting the unloading process and the lifting of the heads off the disk 108. Because the foot 250 of the bent wire 246 protrudes beyond the radius of the disk 108, the bent wire 246 can communicate with the fixed ramp 260 while the head 140 is still loaded onto the disk. As the actuator 110 continues to rotate clockwise, the foot 250 slides up the ramp surface 262 and the rest segment 266

until the actuator 110 and bent wire 246 reach the position illustrated in FIG. 30.

At the point shown in FIG. 30, the actuator 110 is unloaded (as further illustrated in the closeup cross-sectional side view of FIG. 31). Since the actuator 110 has three arms in a preferred embodiment of a disk drive utilizing a two-disk stack, the bent wire 246 of each one of the four suspensions 244 rides up a ramp surface 262 and a rest segment 266.

By way of contrast, the prior art removable cartridge disk drives unloaded heads by moving a non-stationary ramp toward the disk such that a portion of the ramp resides over the disk. The heads can then ride up the ramp to their parked position. Finally, the ramp moves away from the disk to allow the cartridge to be ejected. A moving ramp is required in the prior art removable cartridge disk drive systems to handle two conflicting needs. On the one hand, a ramp must be close enough to the disk to allow the heads to be unloaded onto it before the heads reach the outer diameter of the disk. The clearance tolerances required between the ramp and the disk must be very tight. On the other hand, the ramp must be kept a safe distance away from the disk until a cartridge has been inserted and the disk in the cartridge has settled to a stable position. Otherwise, a bouncing disk could collide with the ramp, thereby damaging the disk and compromising the data and servo information on the disk. As a result, the prior art used a moving ramp which adds cost and complexity to a disk drive. Thus, the bent wire 246 of the present invention advantageously allows the use of a fixed ramp 260 to unload the heads 140 in a removable cartridge disk drive system.

To load the actuator 110 in a preferred embodiment of the present invention, the actuator 110 and the bent wire 246 are rotated counterclockwise from their position in FIG. 30 to their position in FIG. 29. When unloading the heads 140, the voice coil motor 109 rotates the actuator

110 counterclockwise, causing the foot 250 of the bent wire 246 to slide down the rest segment 266 and then the ramp surface 262 of the ramp 260. A closeup cross-sectional side view of this loaded position is further shown in FIG. 32.

The operation of these disk drive components during ejection of a cartridge 101 from the disk drive 100 is as follows. FIGs. 34A-34F illustrate the right side plan view of the progression of parts in the disk drive 100 as the ejection process starts (FIG. 34A) and finishes (FIG. 34F).

Referring to FIG. 34A, the cartridge 101 is in its fully inserted position within the disk drive 100 and the disk drive 100 has not yet commenced the cartridge ejection process. The solenoid 204 is in a non-picked state since the disk drive 101 has not yet started the ejection process, as shown in FIG. 19. Consequently, the plunger 202 is extended out of the solenoid 204 and the solenoid link 200 is in its rest position, as biased by the spring 216.

Referring back to FIG. 34A, the release link 192 is in its non-eject position, here shown as a position parallel to the drive base 106. Accordingly, the release link 192 traps the second end 184 of the catch 180 between the lift plate 194 and safety post 196 of the release link 192. The catch 180 is biased by spring 178 to the position shown in FIG. 34A. Additionally, the slide spring 164 which biases the slide 142 and catch 180 to move toward the drive front end 102 causes the first end 182 of the catch 180 to press against the forward end 190 of the cartridge 101. As explained before, the first end 182 of the catch 180 presses the cartridge 101 against the drive front end 102, thereby locking the cartridge 101 into this fully inserted position. Additionally, the pair of bias springs 220 extending down from the bottom surface of the drive top cover 222 keeps the cartridge 101 resting on the slide 142 and the drive base 106.

When the disk drive 100 is commanded to eject the cartridge, i.e., by a user depressing an eject button on the disk drive 100, the solenoid 204 is electronically picked, resulting in the configuration shown in FIG. 20. The picking of the solenoid 204 retracts the plunger 202, which in turn causes the camming pin 210 to slide in the cam surface 208 of the solenoid link 200. This interaction between the camming pin 210 and the cam surface 208 pulls the solenoid link 200 toward the solenoid 204 and rotates the solenoid link 200 about its pivot pin 214 in a counterclockwise fashion. The counterclockwise rotation of the solenoid link 200 compresses the spring 216 between the solenoid link 200 and the drive base 106.

At this point, the right side view of the disk drive 100 is as depicted in FIG. 34B. The pivoted solenoid link 200 causes the release link 192 to rotate clockwise about its pivot 270 such that the lift plate 194 of the release link 192 engages and carries the second end 184 of the catch 180 upward toward the drive top cover 222. Since the catch 180 is pivotally attached to the slide 142, this upward motion of the second end 184 of the catch 180 causes the catch 180 to rotate counterclockwise so that the first end 182 of the catch 180 dips downward, dropping underneath the forward end 190 of the cartridge 101. Because the first end 182 of the catch 180 no longer prevents the slide 142 from traveling toward the drive front end 102 (as biased by slide spring 164), the slide 142 is free to move toward the drive front end 102.

Referring now to FIG. 34C, the cartridge 101 remains in its fully inserted position. However, since the catch 180 no longer presses against the cartridge 101, the slide 142 and the catch 180 are propelled in their grooves 156, 158 under the cartridge 101 toward the drive front end 102 due to the biasing force created by the stretched slide spring 164 (Fig. 1). At this point in time, the cam nose end 145 of the slide 142 has reached the cam surface 224

in the groove 156. The second end 184 of the catch 180 is no longer retained between the lift plate 194 and safety post 196 of the release link 192. The upward biasing force created by the spring 216 on the solenoid link 200 rotates the solenoid link 200 clockwise to return to the state shown in FIG. 19. The clockwise rotation of the solenoid link 200 rotates the release link 192 counterclockwise about pivot 270, as illustrated in FIG. 34C.

In FIG. 34D, the slide spring 164 has pulled the cam nose end 145 of the slide 142 up the cam surface 224 and out of the groove 156. Since the cartridge 101 rests on the slide 142, the cam nose end 145 of the slide 142 lifts the back end 226 of the cartridge 101 upward toward the cartridge receiver opening 124 in the drive front end 102. At this point in time, the tab 150 of the slide 142 has not yet contacted the forward end 190 of the cartridge 101.

In FIG. 34E, the cartridge 101 is seen reclining at an angle relative to the drive base 106. The slide 142 has now progressed toward the drive front end 102 to the point where the tab 150 of the slide 142 impacts the forward end 190 of the cartridge 101. The impact has sufficient force to launch the cartridge 101 into the interior side of the drive door 120 in the drive front end 102. As shown in FIG. 4, the interior of the drive door 120 has rub rails 132 for the ejecting cartridge 101 to hit. The rub rails 132 prevent the ejecting cartridge 101 from damaging the drive door 120 or any gasket on the drive door 120. Thus, the back end 226 of the ejecting cartridge 101 opens the drive door 120.

The final resting position of the ejected cartridge 101 is as illustrated in FIG. 34F. The impact of the tab 150 on the cartridge 101 is sufficient to eject the cartridge 101 out of the cartridge receiver opening 124 of the drive front end 102, ready to be manually grasped and removed by the user. The slide 142 comes to rest as the

slide spring 164 reaches its relaxed state. Further, a retaining wire 272 shown in FIG. 33 rides in the groove 274 formed in the slide 142. This retaining wire 272 urges the slide 142 toward the drive base 106 and also helps stop the propelled motion of the slide 142 when the retaining wire 272 reaches the end of the groove 274.

Other alternative embodiments of a removable disk drive system involving the insertion and ejection of a cartridge at an angle relative to the drive base are disclosed in a patent application filed concurrently herewith on March 13, 1996 entitled "REMOVABLE CARTRIDGE DISK DRIVE FOR RECEIVING A CARTRIDGE AND METHOD OF INSERTING THE CARTRIDGE," which is fully incorporated herein by reference.

FIGs. 35-37 illustrate top plan views of the removable cartridge 101 as the cartridge door opens. The cartridge 101 has a rounded cartridge forward end 190, a cartridge back end 226, a left wall 276 and a right wall 278, all of which are mounted to a cartridge bottom cover 280 and to a cartridge top cover 282 (not shown in FIGs. 35-37). The cartridge top cover 282 is not been shown in FIGs. 35-37 in order to better highlight the interior features of the cartridge 101. The cartridge forward end 190 is rounded at its corners in accordance with prior art removable cartridge teachings, so that the actuator 110 in the disk drive 100 need not extend as far into the cartridge 101 to load the read/write transducer heads 140. In particular, by removing the corner portions of a cartridge housing as taught in U.S. Patent No. 4,864,452, assigned to SyQuest Technology, Inc., the insertion of an actuator into the cartridge housing is facilitated.

The cartridge 101 preferably encloses a two-disk stack 284 within its confines. The cartridge 101 further has a cartridge door 286 to protect the disk stack 284 from dirt, dust and other contamination. The cartridge door 286 may be a solid vectored or pie-slice shaped door, or a vectored door perpendicularly attached to a band

which covers the opening of the cartridge. The cartridge door 286 has a cartridge door handle 288 having a hooked shape and located at the left forward corner of the cartridge door 286. A cartridge door opening lever 290 of the type well known to those of ordinary skill in the art is pivotally mounted to the bottom surface of the drive top cover 222 (not shown) by a pivot 292. A hooked catch 294 is integrally formed and protruding from the cartridge door opening lever 290. The shape of the hooked catch 294 securely captures the cartridge door handle 288. A spring 296 has one end 297 fixed to the bottom surface of the drive top cover 222. The second end 298 of the spring 296 is hooked around a post 300 extending from the cartridge door opening lever 290.

When the forward end 190 of the cartridge 101 has been inserted sufficiently into the disk drive 100, the hooked catch 294 of the cartridge door opening lever 290 grasps the cartridge door handle 288. As the cartridge 101 is inserted further into the disk drive 100, the cartridge door opening lever 290 rotates clockwise about its pivot 302, shown in FIG. 36, and compresses the spring 296. The clockwise rotation of the cartridge door opening lever 290 causes the hooked catch 294 to pull the cartridge door handle 288 along the same rotation, thereby opening the cartridge door 286 in a clockwise manner (FIG. 36).

When the cartridge 101 is ejected out of the disk drive 100, the progression of components occurs in reverse. The compressed spring 296 urges the cartridge door 286 to close by rotating counterclockwise. As the cartridge 101 is propelled away from the drive back end 103, the cartridge door opening lever 290 rotates counterclockwise and permits the spring 296 to rotate the cartridge door 286 closed. By the time the cartridge 101 ejects out of the disk drive 100, the cartridge door 286 is fully closed.

The cartridge 101 further has an anti-rattle feature whereby the disk 108 is kept from rattling inside the cartridge 101 when the cartridge door 286 is closed, i.e., when the cartridge 101 is not being used. When the cartridge 101 resides inside the disk drive 100 and the cartridge door 286 is open, the disk 108 is released. Two anti-rotation pins 304 are mounted to and extend downwardly from the bottom surface of the cartridge top cover 282 (shown in FIG. 45). Preferably, the anti-rotation pins 304 are formed integrally with the cartridge top cover 282.

The two anti-rotation pins 304 are received by mating holes 306 formed in a cartridge plunger 202 as described in FIGs. 38-40. FIG. 38 depicts a top plan view of the cartridge plunger 308; FIG. 39 illustrates a side view of the cartridge plunger 308; and FIG. 40 is a cross-sectional side view of the cartridge plunger as taken across the section A-A marked in FIG. 38. As is apparent, the cartridge plunger 308 is a circular ring further comprising a top surface 310, a bottom surface 312, a beveled surface 314 and a body 316. The two anti-rotation pin holes 306 for receiving the anti-rotation pins 304 extending down from the bottom surface of the cartridge top cover 282 are formed in the top surface 310 of the cartridge plunger 308. Further, embedded into the interior of the body 316 of the cartridge plunger 308 are three cam riding pins 318 for engaging cam surfaces 320 on a cartridge hub 322 illustrated in FIG. 41.

As shown in the perspective view of the cartridge hub 322 in FIG. 41, the cartridge hub 322 has cam surfaces 320 commencing from the bottom 324 of the cartridge hub 322 and inclining toward the top 326 of the cartridge hub 322. The cam surfaces 320 are also shown in the side view of FIG. 42 and the cross-sectional side view of FIG. 43. The top 326 of the cartridge hub 322 has three mounting prongs 325 for affixing the cartridge hub 322 to the cartridge door 286, the combination of which is shown in FIGs. 35-

37. Thus, the cartridge hub 322 rotates with the cartridge door 286. A torsional spring (not shown) may connect the inside surface of the cartridge hub 322 to a post extending downwardly from the bottom surface of the top cover 282 of the removable cartridge. Rotation of the cartridge hub 322 to the rattle position winds up the torsional spring so that the spring biases the cartridge hub 322 toward the anti-rattle position.

The interaction between the cartridge hub 322 and the cartridge plunger 308 is depicted in the top plan view of FIG. 44. FIG. 44 shows that the bottom 324 of the cartridge hub 322 mates with the top surface 310 of the cartridge plunger 308. The cam riding pins 318 of the cartridge plunger 308 ride the cam surfaces 320 of the cartridge hub 322. As the cam riding pins 318 ride further up the cam surfaces 320 toward the top 326 of the cartridge hub 322, the cartridge plunger 308 fits more snugly against the cartridge hub 322. When the cam riding pins 318 are descending the cam surfaces 320 away from the top 326 of the cartridge hub 322, the gap between the cartridge plunger 308 and cartridge hub increases. Thus, as will be discussed in greater detail later, the overall height of the combination of the cartridge plunger 308 and the cartridge hub 322 decreases when the cam riding pins 318 travels up the cam surfaces 320 and increases when the cam riding pins 318 rides down the cam surfaces 320.

FIG. 45 is a see-through cross-sectional side view of the cartridge 101 and depicts the interaction between the cartridge plunger 308, cartridge hub 322 and the rest of the cartridge 101. The cartridge 101 has a disk pack 327 which comprises two disks 108, a cartridge disk hub 328 for mounting to the disk drive spindle motor 107, a spacer 330 for separating the two disks 108, a flexure 332 which acts as a spring between the disk 108 and the cartridge bottom cover 280, an armature plate 334 which acts as a magnetic chuck to engage the disk drive motor 107, and rivets 336 to hold various cartridge components together.

FIG. 45 shows the position of these cartridge components when the anti-rattle mode is activated. The cartridge top cover 282 has descending therefrom two anti-rotation pins 304. These two anti-rotation pins 304 extend into the two anti-rotation pin holes 306 formed in the cartridge plunger 308. As the cam riding pins 318 of the cartridge plunger 308 ride down the cam surfaces 320 of the cartridge hub 322 (i.e., towards the cartridge bottom cover 280), the cartridge plunger 308 moves further from the cartridge hub 322 (and the cartridge top cover 282) because the anti-rotation pins 304 serve to translate the rotational force generated by the camming motion into vertical movement of the cartridge plunger 308 relative to the cartridge hub 322. The movement of the cartridge plunger 308 away from the cartridge hub 322 and closer toward the cartridge bottom cover 280 eventually causes the beveled surfaces 314 of the cartridge plunger 308 to engage and press upon the cartridge disk hub 328 at the contact radius 338. Furthermore, the flexure 332 is compressed between the disks 108 and the cartridge bottom cover 280. Thus, the downwardly biased cartridge plunger 308 presses the disk pack 327 against the cartridge bottom cover 280 at contact radiuses 338 and 340, thereby preventing the rattling of the disks 108.

The release of the anti-rattling mode of the cartridge 101 is described next. In FIG. 45, as the cam riding pins 318 of the cartridge plunger 308 ride up the cam surfaces 320 of the cartridge hub 322 (i.e., towards the cartridge top cover 282), the cartridge plunger 308 travels closer to the cartridge hub 322 (and cartridge top cover 282) and the anti-rotation pins 304 extend further into the two anti-rotation pin holes 306 of the cartridge plunger 308. The upward motion of the cartridge plunger 308 toward the cartridge top cover creates gaps at contact radiuses 338 and 340, thereby allowing the disk pack 327 to rattle inside the cartridge 101.

The anti-rattle mode is desirable when the cartridge 101 is not in use since rattling of the disks when a user is transporting the cartridge 101 may damage the disks' surfaces (or at least instill fear in the user that such damage is occurring). By contrast, the anti-rattle mode must be disengaged when the cartridge 101 is in use so that the disk pack 327 can spin freely at high revolutional speed. This selective engagement and disengagement of the cartridge's anti-rattle feature is accomplished by the position of the cartridge door 286, as is illustrated in the sequence of FIGs. 35-37.

As previously stated, the cartridge door 286 is mounted to the top 326 of the cartridge hub 322. Thus, when the cartridge door 286 is closed (FIG. 35), the cam riding pins 318 of the cartridge plunger 308 are oriented such that they reside at the bottom of the cam surfaces 320 of the cartridge hub 322. As a result, the cartridge plunger 308 is at its furthest position from the cartridge hub 322, thereby compressing the disk pack 327 against the cartridge bottom cover 280 (i.e., the anti-rattle mode).

When the cartridge door 286 is opened by the cartridge door opening lever 290 of the disk drive 100, the cam riding pins 318 of the cartridge plunger 308 travel up the cam surfaces 320 of the cartridge hub 322, pulling the cartridge plunger 308 up toward the cartridge top cover 282. When the cartridge door 286 is fully opened (or near fully opened), the cartridge plunger 308 releases the disk pack 327.

<u>Burst In Range and Special Data Sector Modes</u>

The disk drive uses a Burst In Range mode and a Special Data Sector mode to enhance the drive's servo error handling, as discussed in greater detail below. The Burst In Range mode and the Special Data Sector mode enable the drive to perform read, write and disk formatting functions more advantageously, accurately and efficiently.

Formatting is that process during which information such as headers are written to the disk so that data sectors are identifiable and usable by the disk drive's read and write software which in turn are employed as logical data storage entities by the host computer. The formatting process must deal with concerns that are not usually faced by ordinary writing to a disk. For example, the formatting process writes headers to a disk having prerecorded servo fields and thus, must be sure of the location of servo fields so as to not overwrite any part of the servo fields. Ordinary writing to a formatted disk is simpler in that the disk has headers and other information that help the drive more accurately locate servo fields and data sectors. The invention permits the formatting process, the error handling process, and their implementations in software and/or hardware to be more efficient, accurate and faster executing.

The implementation of these modes involves the use of the disk drive's microprocessor, software executed by the microprocessor, an ASIC (Application Specific Integrated Circuit), and a sequencer or interface controller chip made by Adaptec, Inc. which is an AIC-8321 for IDE-interfaced disk drives and an AIC-8371 chip for SCSI interfaced disk drives. The ASIC has circuitry that performs four functions of particular interest: (1) dual interrupt status registers, (2) interrupt mask, (3) burst in range mode hardware and (4) special data sector mode hardware.

The disk drive software that is executed by the microprocessor is composed of multiple sub-programs that run as independent software processes that are time sliced to execute concurrently. The two major processes of particular interest are the "drive interface process" and the "servo process." Both of these processes need to read error statuses from the ASIC.

The drive interface process is concerned with the formatting of, writing to and reading from the disk and

requires error statuses because the process must know whether it is unsafe to proceed with these activities. Thus, the drive interface process needs to acquire error statuses relative to specific data sectors but does not need to acquire error statuses after every servo field. The drive interface process is also selective about which error statuses are to be reported to the microprocessor because some error conditions may be deemed inconsequential during certain circumstances.

The servo process requires information about the head position error relative to the track centerline (i.e., the off track error shown in FIG. 47) so that the servo process can correct the head position as needed. Hence, the servo process requires error statuses to be updated subsequent to every sample of a servo field.

Burst In Range Mode

During the formatting of a disk, it is desirable for the drive to stop writing to the disk upon the occurrence of certain error conditions. Thus, the disk drive of the present invention enters a Burst In Range mode just before formatting a disk. While the invention may be used during ordinary writing to the disk, the invention is particularly advantageous for formatting processes. The Burst In Range mode causes the drive to inhibit writing to the disk if (1) the position of the read-write head is within the desired range of data sectors to be written to and (2) an error condition is detected and that error condition is a type of error allowed to pass through a mask circuit. The Burst In Range mode operates structurally and functionally as follows:

The ASIC contains two interrupt status registers, one for the servo process (the "servo error status register") and the other for the drive interface process (the "drive interface status register"). FIG. 46 is a simplified block diagram that shows conceptually the servo error status register 400, a mask circuit 402 (which may be implemented as a register), the drive interface status

register 404 and logic circuitry blocks 406 which are used to implement a Burst In Range mode in a disk drive. These circuits are located in the ASIC.

A servo error detection circuitry which may be one of the various servo error detection circuitries known in the art detects servo errors as the read/write transducer heads 140 fly over servo sectors on the disk 108. Upon the detection of error conditions, the servo error detection circuit generates an error status bit 401 for each error condition found. Each error status bit 401 represents a type of error condition. Examples of these types of error conditions include but are not limited to: preamplifier write unsafe, write unsafe, cylinder error, shock error, missed servo synchronization mark, off track error, spin speed error, bad grey code and missing servo burst. Each error status bit 401 is passed from the servo error detection circuitry to a servo error status register 400. A detected error condition causes at least one error status bit 401 to be written into the servo error status register 400.

The servo error status register 400 passes its error status bits to the mask circuit 402. The mask circuit 402 masks out certain error status bits, thereby preventing masked error status bits from passing through the mask circuit 402 to the drive interface status register 404, while permitting unmasked error status bits 403 to pass through to the drive interface status register 404. In actual implementation, the unmasked error status bits are converted into count values which are then sent to the drive interface status register 404. The count values permit the disk drive to have an error history feature as will be described in greater detail below. Reference numeral 403 thus refers to either unmasked error status bits or unmasked error statuses that have been converted into count values, depending if an error history feature is implemented or not. Therefore, not every error status bit 401 is necessarily sent to the drive interface status

register 404 (although every bit could be sent). Whether a particular error status bit corresponding to an error condition is masked out depends on the contents of the mask circuit 402 corresponding to that error condition.

An error status bit 401 is passed to the drive interface status register 404 (during the Burst In Range and Special Data Sector modes) if and only if the error status bit 401 satisfies two conditions: (1) the error condition corresponding to that bit occurred during the access of a data sector that was to be read from or written to, and (2) the type of error condition was one should trigger the disk drive to interrupt the read/write operation of a data sector. Hence, the presence of one or more error status bits 403 in the drive interface status register 404 indicates to the disk drive that an error condition has occurred, that the error condition was not masked out by the mask circuit 402 and that a data sector may need to be re-accessed in order to assure the integrity of the attempted process.

The disk drive uses an interrupt system to convey error statuses from the drive interface status register 404 to the microprocessor. The ASIC periodically sends an interrupt signal to the microprocessor so that error statuses can be reported to the microprocessor. For example, in response to the interrupt signal, the microprocessor may read the error status relating to head position error from the ASIC and act upon the information to correct the error.

FIG. 47 illustrates in greater detail an implementation of the conceptual, simplified circuitry shown in FIG. 46. The servo error status register 500 is illustrated as a column of flip flops 502-508. These flip flops 502-508 may be any kind of flip flops such as D flip flops or Set-Reset (SR) flip flops. The drive interface status register 510 is shown as a column of D flip flops 512-519. In the middle of FIG. 47, a mask circuit 520, which is comprised of a column of mask counters 522-528,

resides between the servo error status register 500 and the drive interface status register 510.

The flip flops 502-508 of the servo error status register 500 receive error status bits 401 from the servo error detection circuit about error conditions and pass those error status bits 401 to the mask circuit 520. The microprocessor uses the Read Servo Status signal 530 to read the contents of the servo error status register 500 and then clear the register.

When the mask circuit 520 receives an error status bit 401 from the servo error status register 500, the mask circuit 520 loads a particular count value that the microprocessor transferred to the mask count register 532 over line 533. Each type of error condition is assigned to a certain count value by the software. An error status bit 401 causes a corresponding mask counter 522-528 of the mask circuit 520 to load the count value corresponding to the error condition (and as stored in the mask count register 532) into the mask counter.

The detection of a servo synchronization mark in each servo field causes the Servo Interval line 534 to decrement each mask counter 522-528 by one. If a mask counter 522-528 has already been decremented to zero, the counter does not decrement any further. Thus, the loading of a count value into the mask counter coupled with the decrementing of the mask counter when a servo sector is detected provides the disk drive with a recent history of error conditions. Each applicable type of error condition is allotted a 2-bit or 3-bit count value to count the number of servo sectors that have passed since the last occurrence of that error. From the drive interface status register 510's point of view, a particular error condition is active not only during the servo sector of its occurrence, but also during subsequent servo sectors during which time the respective mask counter contains a non-zero value. Thus, each error condition is "remembered" for the time period it takes a read-write

head to pass over the number of consecutive servo sectors equal to the count value. As can be seen by the input lines to mask counters 527 and 528 in FIG. 47, off-track errors and spin speed errors are given a three bit count value, while the other errors are assigned only a two bit count value. The three bit count values enable the disk drive to remember off-track errors and spin speed errors for a longer amount of time so that the drive has more time to take corrective measures such as to wait a settling time for the error conditions to dissipate. These relative count values are shown for illustrative purposes only and are not intended to limit which types of error conditions are "remembered" longer than other types of error conditions.

The mask circuit 520 continues to pass an error status bit 401 to the logic gates 536-549 until the count value associated with that error condition has been decremented to zero. When a mask counter reaches a value of zero, it stays at zero for each subsequently detected servo sector. The only way for a mask counter to acquire a non-zero value is to be loaded in response to a detected error condition. A mask counter that contains a zero value presents no error status to the drive interface status register 510 because the time duration that the error condition was to be remembered has expired.

If the count value to be loaded into a mask counter 522-528 from the mask count register 532 is already zero, the zero value means that the masking circuit 520 has masked out (or ignored) the existence of that error condition because the error condition will be remembered for a zero length of time. For example, the micro-processor can write a count value of zero into mask count register 532 in order to ignore bad grey code error conditions.

If a count value is loaded into a mask counter 522-528 and the same error is detected again during the next servo sector, the procedure repeats, meaning that the

count value is re-loaded into the mask counter and the mask counter is not decremented. Thus, the length of time that an error condition is remembered by a mask counter 522-528 is based on the last time that the error condition occurred during a consecutive series of detection of the same error.

FIG. 48 illustrates a (not to scale) representation of a portion of a track 558 on a disk having servo sectors 560 that comprise servo fields 562 and data sectors 564 (which may include split data sectors 566). Each servo field 562 has a servo burst pattern that includes a servo synchronization mark at the beginning of the servo field 562. Servo synchronization mark pulses 568 represent the presence of these servo synchronization marks. A servo sector is the interval on the disk lying between two consecutive servo synchronization marks. A data sector is that part of a track which contains the minimum unit of user data, for example, 512 bytes. The servo fields 562 are conceptually illustrated as small vertical blocks and the data sectors 564 as the large horizontal blocks.

Servo sectors 560 and data sectors 564 are assigned identifying numbers relative to the index mark on the track. The particular numbers chosen for FIG. 48 were selected arbitrarily, but lie within the range of numbers actually encountered on a disk track. Servo sectors 560 are identified by a unique number assigned to the servo sector 560 which is a number equal to the sector's offset from the index mark on the track. Thus, servo sectors 560 are identified by a number ranging from 0 to some maximum number which is one less than the number of servo sectors on a track. In the actual implementation, servo sector numbers range from 0 to 59, and data sector numbers are variable depending on the radial distance of the track from the center of the disk. As shown, servo fields 562 (servo field numbers 5-9) are interspersed in data sectors 564 (data sector numbers 14-26). Some data sectors 566 (i.e., data sector numbers 17, 22 and 24) are split by

servo fields 562 (servo field numbers 6, 8 and 9 respectively) and handled by the sequencer chip.

Servo fields 562 are detected by a servo demodulator circuit in the ASIC which may be of any type well known to those of ordinary skill in the art. The disk drive determines the location of data sectors 564 by first detecting the relevant servo field 562, finding the servo synchronization mark 568 in the servo field 562, and determining the offset at which the data sector 564 is located from the servo synchronization mark 568. The offsets are determined by a software algorithm well known to those skilled in the art.

FIG. 48 further has a timing diagram with four waveforms that depict how the mask counter circuitry enables the disk drive to remember an error condition for a programmable number of servo sectors after the passing of the servo sector with the error condition.

The first waveform illustrates servo synchronization mark pulses 568 over time; the second waveform depicts the contents of the servo error status register 500; the third waveform shows the contents of the count value stored in the relevant mask counter 522-528; and the fourth waveform illustrates whether the error condition is reported to the drive interface status register 510.

FIG. 48 presents an example operation of an error condition being detected during servo sector number 6. Prior to servo sector number 6, no error status bits have been set in the servo error status register 500 as indicated by the term "clear" in the second waveform of FIG. 48. The error condition detected in servo sector number 6 by the servo error detection circuitry is latched into the servo status register 500 as an error status bit 401. At the same time, the mask count register 532 loads a count value of "3" into the mask counter corresponding to the error condition as shown in the third waveform. Thus, the disk drive is to remember the detected error condition for three servo sectors. If multiple error

conditions were detected during servo sector number 6, a multiplicity of mask counters would be loaded with count values simultaneously.

Prior to the occurrence of servo sector number 7, the microprocessor clears the error status bit(s) 401 latched in the servo error status register 500. The microprocessor clears the servo error status register 500 when the microprocessor uses the Read Servo Status line 530 to read the contents of the servo error status register 500.

As shown in FIG. 48, the mask counter is decremented relative to the servo synchronization mark 568 found in each of servo sector numbers 7, 8 and 9. The fourth waveform shows that the detected error condition is reported to the drive interface status register 510 for three servo sector times. The fourth waveform further shows that the detected error condition is sent to the drive interface status register 510 during servo sector numbers 6, 7 and 8 even though the error condition is no longer asserted in the servo error status register 500 during servo sector numbers 7 and 8. When the count value has been decremented to zero (i.e., after servo sector number 9), the error condition is no longer reported to the drive interface status register 510. Once the mask counter has been decremented to zero, it remains at zero until the mask count register loads another count value into the mask counter.

Returning to FIG. 47, not all error conditions detected during the Burst In Range mode are reported to the drive interface status register 510 for three reasons. First, error conditions detected during data sectors not of interest may not be relevant. The state of a Burst In Range ("BIR") bit 408 indicates whether data sectors being accessed are data sectors of interest. Thus, a reset BIR bit 408 instructs the logic gates of FIG. 47 to ignore any error status bits 401 received from the mask circuit 520 since the error conditions relate to data sectors that are

not of interest. A set BIR bit 408 tells the logic gates 536-549 that the detected error condition relate to data sectors of interest. Second, some error conditions or combinations of error conditions may be deemed inconsequential under certain circumstances. The mask circuit 520 in conjunction with the mask count register 532 select which error statuses to report to the drive interface status register 510, which in turn, reports error statuses to the microprocessor. Inconsequential error statuses are masked out, as described above. Third, the drive interface process is interested in the first servo error condition to be passed through the mask circuit 520 to the drive interface status register 510 and ignores successive errors in time since the occurrence of a single error triggers error handling regardless of how many other errors also occur.

Therefore, whether the drive interface status register 510 is updated with new error statuses (or their corresponding count values) depends on the state of the BIR bit 408 and whether the register 510 already indicates the existence of an error condition (i.e., presence of one or more asserted error status bits in the register). Logic gates 536-549 receive count values corresponding to error statuses from the mask circuit 520 and pass the count values to the drive interface status register 510 if the BIR bit 408 is set. The drive interface status register 510 may be updated with new error statuses if the BIR bit 408 is enabled and if the register 510 does not already indicate the existence of an error condition.

The NOR gate 552 in FIG. 47 disables the logic gates 536-549 from sending error status bits (or their corresponding count value bits) 403 to the drive interface status register 510 if at least one error status bit has already been set in the register 510. The register 510 may not be updated if the BIR bit 408 is disabled, or when the register 510 already indicates that an error condition exists regardless of the state of the BIR bit 408.

Therefore, during the Burst In Range mode, only the first error condition that is not masked out by the mask circuit 520 is saved in the drive interface status register 510. Once the drive interface status register 510 indicates that an unmasked error condition has been detected during Burst In Range mode, subsequent error conditions are ignored.

FIG. 49 has timing diagrams that illustrate the operation of the Burst In Range mode. Timing diagrams are provided for the Sequencer Input/Output ("SEQ I/O") line 570, Unsafe Enable Bit 572 and BIR bit 408 and the contents of the drive interface status register 510 before and during the Burst In Range mode. Points A-F indicate events of particular interest.

Before activating the Burst In Range mode, the following initialization must occur. First, the SEQ I/O line 570 from the sequencer to the ASIC is cleared to 0, as shown in Event A of FIG. 49. The sequencer sends a signal on its SEQ I/O line 570 to notify the ASIC whether the data sectors being accessed currently by the read-write heads 140 are within a certain range of the target data sectors, or in other words, "data sectors of interest." The cleared SEQ I/O signal 570 indicates that the data sector under the read-write head is not within a certain range of the target data sector.

Event B of FIG. 49 shows the software resetting an Unsafe Enable Bit 572 which is a bit residing in a microcontroller-addressable register space in the ASIC. The resetting of the Unsafe Enable Bit 572 to "0" causes the ASIC to reset the BIR bit 408 to "0."

Event C of FIG. 49 shows the software setting the Unsafe Enable Bit 572 back to "1." The high-going transition of the Unsafe Enable Bit 572 from 0 to 1 causes the drive interface status register 510 to be cleared of error statuses (as shown in the third waveform) so that no error conditions are deemed to exist at the start of the Burst In Range mode. Now that the BIR bit 408 and the

drive interface status register 510 have both been initialized (i.e., cleared), the Burst In Range mode is ready to start, though not yet activated.

The Burst In Range mode is activated when the sequencer determines that the data sectors being accessed currently by the read-write heads 140 are within a certain range of the target data sector to be formatted. Although the ASIC knows which servo sector has passed under the read-write head, the ASIC relies on the sequencer to determine whether a target data sector has passed under or within a particular range of the read-write head. The sequencer determines if the read-write head is within range of the target data sector by using an algorithm well known in the art to count off data sectors as they pass under the read-write head.

Turning to Event D of FIG. 49, the sequencer sends a 1 signal on its SEQ I/O line 570 to the ASIC when the read-write head is within range of the target data sector. The transition from 0 to 1 on the SEQ I/O line 570 signifies to the ASIC that the read-write heads 140 are now within a certain range of the target data sectors. When the ASIC detects this transition on the SEQ I/O line 570, the ASIC activates the Burst In Range mode by setting the BIR bit 408 inside the ASIC. The BIR bit 408 propagates to the logic gates 536-549 in FIG. 47 (or the logic circuitry 406 in FIG. 46) to permit detected error status bits 403 to pass from the mask counters 522-528 to the drive interface status register 510.

Event E of FIG. 49 depicts the detection of the first error condition. Assuming that this first error condition is not masked out by the mask circuit 520, the error condition is reported to the drive interface status register 510 because the BIR bit 408 is set and the drive interface status register 510 contains no error status bits.

Event F of FIG. 49 shows that subsequently detected error conditions are ignored and not reported to the drive

interface status register 510. Error conditions are ignored until Events A-C are repeated.

Once the Burst In Range mode is activated, the drive may write to the disk until an error condition that is not masked out by the mask circuit 520 is detected. The detection of the first unmasked error condition signals a safety circuit 574 (FIG. 51) to turn off the write current to the read-write head, thereby inhibiting writing to the disk. The safety circuit 574 may be a circuit well known in the art to turn on and off write current. If a servo error condition is detected while the ASIC is in Burst In Range mode, the safety circuit 574 continues to inhibit writing to the disk until the software re-starts the Burst In Range mode by re-executing the requisite series of steps described above.

Special Data Sector Mode

When the drive interface status register 510 indicates the existence of an error condition, the disk drive needs to identify the data sector during which the error occurred and re-access the potentially compromised data sector(s). The data sectors preceding the servo error can be transmitted to the final destination (the host computer or the disk) as these data sectors are error-free (as far as the relevant types of error conditions are concerned). Prior art disk drives, however, could not pinpoint exactly which data sector had the servo error and thus, had to back up to some selected data sector beyond the actual data sector having the error condition in order to ensure that the data sectors being read or written are valid.

FIG. 50 illustrates a representation of a portion of a track on the disk and four waveforms showing the operation of the Special Data Sector mode. When a drive is ready to format a disk, the drive must spin the disk and read the servo fields 562 as they pass under the read-write head until the drive finds the servo sector containing the target data sectors. That servo sector is

the target servo sector. During reading or writing to the target data sectors, error conditions may be detected and recorded into the drive interface status register 510. At this point, prior art disk drives were unable to determine the precise data sector during which the error condition occurred and resorted to backing up beyond the actual data sector having the error. The disk drive of the present invention, on the other hand, can determine the exact data sector during which the error arose and thus, simply and efficiently reprocesses from that data sector forward. To do so, the disk drive invokes a Special Data Sector mode to locate the precise data sector during which an error condition arose.

The example represented by FIG. 50 assumes that the initialization phase of the Special Data Sector mode has been executed and that the target servo sector is servo sector number 6 such that when the system detects the servo field 562 corresponding to the number 6, the system activates the Special Data Sector mode.

The ASIC has a sector pulse generation logic 578 (shown in block diagram form in FIG. 52) of a design well known in the art. The sector pulse generator 578 in FIG. 50 generates a sector mark pulse 580 for every data sector of interest 564 detected under the read-write head. The data sectors of interest in FIG. 50 are shown to arbitrarily start at data sector number 18. Each sector mark pulse 580 is actually generated relative to a specific offset added to the location of the servo synchronization mark 568. As can be seen in FIG. 50, these offsets cause the sector mark pulses 580 to line up with the occurrence of data sectors 564.

The Special Data Sector mode controls whether the sector pulse generator 578 generates sector mark pulses 580 upon the detection of each data sector 564. If the Special Data Sector mode is enabled, the sector pulse generator 578 issues a sector mark pulse 580 for every data sector 564. If the Special Data Sector mode is

disabled, the sector pulse generator 578 does not generate sector mark pulses 580. In operation, the drive disables the Special Data Sector Mode to inhibit sector mark pulse generation until the target servo sector passes under the read-write head. In the example of FIG. 50, the target servo sector is servo sector number 6. Thereafter, the Special Data Sector mode is enabled so that sector mark pulses 580 are generated until an error condition passed through the masking circuit 520 is detected.

To execute the Special Data Sector mode, the system must perform the following steps: (1) inhibit the generation of sector mark pulses 580, (2) determine the identifying number of the target servo sector 560, and (3) activate the Special Data Sector Mode. To accomplish the first step, the microprocessor sets an inhibit_sector_pulse register bit 582 in the ASIC which inhibits the sector pulse generator 578 from generating sector mark pulses 580. To accomplish the second step, the microprocessor writes the identifying number associated with the target servo sector 560 into a target_servo_sector register 586 (shown on FIG. 55) in the ASIC. The identifying number of the first target data sector is written into two registers in the ASIC: the Last Data Sector Number (LDSEC) register 583 and the Burst Data Sector Number (BDSEC) register 584. The ASIC has a BRSTNMB counter 588 (FIG. 53) that is cleared upon the index mark and counts up for every servo sector 560 that passes under the read-write head. A comparator 590 (FIG. 54) in the ASIC compares the target identifying number on line 592 from the target_servo_sector register 586 with the BRSTNMB counter 588's identifying number of each servo sector 560 that passes under the read-write head and outputs a control signal when the two values are equal, thereby indicating when the read-write head has reached the target servo sector. At this point in time, the Special Data Sector Mode should be activated. The third step is accomplished when the microprocessor sets a

Special Data Sector mode bit 581 (FIG. 54) which allows the control signal from the comparator 590 to activate the Special Data Sector mode. Although one particular circuit embodiment is described, numerous alternative circuit configurations may be used. These register bits and counters can also be implemented in a variety of ways of storing information.

With the Special Data Sector mode activated, sector mark pulses 580 are generated for all data sectors 564 arriving after the servo synchronization mark 568 in the target servo sector. In the example of FIG. 50, sector mark pulses 580 begin to be generated at data sector number 18. Sector pulse generation continues as long as no error conditions are detected and recorded in the drive interface status register 510. If an error condition is recorded into the drive interface status register 510, an error condition was detected during the processing of a data sector of interest and the error condition was deemed by the mask circuit 520 to be of a type that may jeopardize writing to the disk.

Once the read-write head is within range of the target data sectors, the LDSEC register 583 maintains the identifying number of the data sector that most recently passed under the read-write head. Each sector mark pulse 580 causes the LDSEC register 583 to be updated to the identifying number of the next data sector. When a servo synchronization mark 568 is detected, the BDSEC register 584 is updated with the identifying number of the last data sector to have passed under the read-write head (i.e., the number stored in the LDSEC register 583) when the servo field was detected.

An example of the operation of the Special Data Sector mode is shown in FIG. 50. The timing diagram with four waveforms in the lower half of FIG. 50 represent significant activities which transpire prior to, during, and immediately after the Special Data Sector mode's active interval. The waveforms in FIG. 50 show the

behavior of sector mark pulses 580 and the contents of the LDSEC and BDSEC registers 583, 584 during the Special Data Sector mode. The first waveform represents pulses generated at detection of servo synchronization marks 568 that lie at the beginning of each servo field 562. The second waveform represents sector mark pulses 580 generated by the sector pulse generator 578 at locations equal to various offsets from the servo synchronization marks 568. The third and fourth waveforms show the contents of the LDSEC register 583 and the BDSEC register 584 respectively during the passage of the Special Data Sector mode. As can be seen, the number stored in the LDSEC register 583 is the identifying number of the data sector last detected, and the number stored in the BDSEC register 584 is the number in the LDSEC register 583 at the moment a servo synchronization mark 568 is detected.

In particular, when the third servo synchronization mark 568 (reading from left to right) is detected, the LDSEC register 583 contains "19" and the BDSEC register 584 is updated from "17" to "19." When the fourth servo synchronization mark 568 is detected, the LDSEC register 583 contains "22" and the BDSEC register 584 is updated from "19" to "22." Lastly, when the fifth servo synchronization mark 568 is detected, the LDSEC register 583 contains "24" and the BDSEC register 584 is updated from "22" to "24." At this point in time, FIG. 50 assumes that an error condition was detected during servo field number 9 and recorded into the drive interface status register 510. The detection of the error condition immediately deactivates the Special Data Sector mode, which in turn inhibits the generation of sector mark pulses 580. Because sector mark pulses 580 are no longer generated, the LDSEC register 583 cannot change its contents to the identifying numbers of other data sectors as the LDSEC register 583 has no way of knowing when a data sector 564 has been detected without the sector mark pulses 580. The content of the BDSEC register 584 which

gets its value from the LDSEC register 583 also does not change since the LDSEC register 583 is frozen. As a result, the two "frozen" registers 583, 584 contain the identifying number of the data sector during which the servo error occurred and the identifying number of the last data sector in the servo sector to occur before the error occurred, respectively. In this particular example, the two values are the same, although they could be different. Both the Special Data Sector Mode and the drive interface status register 510 are reset only after execution of the steps described above.

In summary, the Burst In Range Mode and the Special Data Sector Mode provide two services, either singly or concurrently. The functions performed by each mode are distinct, yet related, as summarized below.

The Burst In Range Mode is activated when the sequencer issues a timed pulse to the ASIC to indicate that the read-write head is within a certain range of the target data sectors to be written to. The Burst In Range mode allows write current to be driven into the read/write head and immediately turns off the write current upon occurrence of certain unmasked error conditions. This operation prevents writing to the disk when accurate writing cannot be assured.

The Special Data Sector mode is activated when the ASIC determines that the target servo sector has passed under the read-write head. Activation of the mode allows sector mark pulses 580 to be generated which are passed to the sequencer to identify data sectors 564 on the disk. During the Special Data Sector mode, sector mark pulses 580 are generated until certain unmasked error conditions occurs, at which point sector mark pulses 580 are immediately inhibited. The contents of the LDSEC and BDSEC registers 583, 584 reveal the exact data sector 564 during which the error condition occurred. This mode accurately and efficiently locates the precise data sector 564 that needs to be reprocessed. All data sectors 564

accessed starting with this data sector must be re-accessed.

FIGs. 51-63 illustrate detailed circuitry which performs a variety of tasks, including the circuitry used to implement a Burst In Range mode and a Special Data Sector mode. While FIGs. 51-63 describe a particular embodiment of the invention in greater detail, the invention can be implemented in many ways as would be apparent to one of ordinary skill in the art. By convention, inputs to a block of circuitry are shown to the left of the block and outputs from a block are drawn to the right of the block. FIGs. 51-63 are first discussed at a high level and then the significant signals and circuits used to implement the Burst In Range and Special Data Sector modes will be discussed.

FIG. 51 depicts a top level diagram of major constituent components in the ASIC used to implement a Burst In Range mode and a Special Data Sector mode. In particular, K21INT block 600 contains the servo error status register 500, drive interface status register 510 and mask circuit 520, as well as LDSEC register 583, BDSEC register 584, an interrupt circuit 601, an interface to the microprocessor bus and other circuits.

SECTPEQ2 block 602, safety circuit 574, gray code decoder 606 and a serial interface circuit 608 are shown in block diagram form. SECTPEQ2 block 602 contains the Burst In Range (BRSTRNG) logic 610 (shown in FIG. 53), sector pulse generator 578 (FIG. 52) and some ancillary circuitry. The safety circuit 574 turns on and off write current to the read-write heads. The gray code decoder 606 decodes gray codes. The serial interface circuit 608 permits the ASIC to communicate with other chips through a serial communications protocol.

FIG. 52 illustrates the detailed circuitry within the SECTPEQ2 block 602 of FIG. 51. SECTPEQ2 block 602 includes SECTOR2 block 612, MODULON block 614, SEARCHGN block 616 and sector pulse generator 578. Sector pulse

generator 578 generates sector mark pulses 580 for every data sector detected during the Special Data Sector mode. SECTOR2 block 612 serves as part of the servo error detection circuit by detecting certain errors, such as the spin speed error and missed servo synchronization mark error. SECTOR2 block 612 further contains a BRSTNMB counter 588 (shown in FIG. 53) that provides the identifying number of the most recently detected servo sector on bus 619 to Burst In Range (BRSTRNG) logic 610 so that the BRSTRNG logic 610 can activate the Burst In Range mode when the read-write head is within range of the target data sector. SEARCHGN block 616 defines a window during which a servo field is expected to be detected. During this window, the servo demodulator circuit in the ASIC looks for servo fields. MODULON block 614 contains counters used to help servo pulse generator 578 generate servo mark pulses 580 on a zone recorded disk. The Burst In Range and Special Data Sector modes work with but do not require zone recording.

FIG. 53 shows the detailed circuitry within SECTOR2 block 612 of FIG. 52. Of particular interest is Burst In Range (BRSTRNG) circuit block 610 which resets the BIR bit 408 prior to activation of the Burst In Range mode and sets the BIR bit 408 when the Burst In Range mode is to be activated. Comparator 590 on FIG. 54 compares the number of the target data sector with the data sector under the read-write head as sent over bus 619. When the target has been reached, the comparator 590 permits the activation of the Burst In Range mode. BRSTCNTA block 620 measures the distance between servo fields and based upon the distance between detected servo fields, determines the existence of spin speed errors and missed servo synchronization mark errors.

FIG. 54 illustrates the detailed circuitry within the Burst In Range circuit block 610 of FIG. 53. FIG. 55 depicts circuitry in the K21INT block 600 of FIG. 51 including INTERPT block 601, target_servo_sector register

586 and some ancillary registers. FIGs. 56-63 illustrate circuitry inside INTERPT block 601 of FIG. 55. In particular, FIG. 56 shows the servo error status register 500, drive interface status register 510 and logic circuitry 406; FIG. 57 shows the mask count register 532; FIG. 58 illustrates the mask counters comprising mask circuit 520; FIG. 59 depicts the LDSEC register 583; FIG. 60 shows the BDSEC register 584; and FIGs. 61-63 illustrate three-bit and two-bit counters which are used to implement mask counters 710, 719 and 720 respectively in FIG. 58.

To initialize the system to start the Burst In Range mode as previously described, the following occurs in FIGs. 51-61. The sequencer determines whether the read-write head is within a certain range of the target data sector to be formatted and notifies the ASIC with a signal on the SEQ I/O line 570 which eventually reaches the K21INT block 600 of the ASIC in FIG. 51. When the ASIC learns from the sequencer that the read-write head is within range of the target data sector, the K21INT block 600 passes a "1" signal on its SEQ I/O line 570 to the SECTPEQ2 block 602. The SEQ I/O signal 570 passes to the SECTOR2 block 612 in FIG. 52. Inside the SECTOR2 block 612 as illustrated by FIG. 53, the SEQ I/O signal 570 enters the BRSTRNG block 610, which is shown in greater detail in FIG. 54. The SEQ I/O signal 570 enters D flip flop 624 which generates SEQIOX 626 and its complement NSEQIOX 628 as 1 and 0 respectively if the read-write head is within range of the target data sector and as opposite values if the read-write head is out of range. Prior to the Burst In Range mode, the read-write head is assumed to be out of range of the target data sector so SEQIOX 626 and NSEQIOX 628 are 0 and 1 respectively.

The ASIC sends a 0 to the D flip flop 629 via the Unsafe Enable Bit (12C9) line 572. In response, the D flip flop 629 resets UNSAFEN 630 to 0 and sets its complement NUNSAFEN 632 to 1. Having initialized the

UNSAFEN 630, the ASIC sends a 1 on Unsafe Enable Bit line 572 to the D flip flop 629 to set UNSAFEN 630 to 1 and NUNSAFEN 632 to 0. Logic 634, logic 636 and logic 644 (which generates U1 640 and U0 641) comprise logic that sequences through the Burst In Range mode and may be implemented in a wide variety of ways. UNSAFEN 630 and its complement NUNSAFEN 632 are received by logic 634. As discussed above, NSEQIOX 628 is presently 0 because the read-write head is not yet within range of the target data sector. As a result, the high-going transition of UNSAFEN 630 from 0 to 1 causes logic 634 to switch NCLRBIR 642 from 0 to 1. The high-going transition on NCLRBIR 642 causes logic 636 which includes D flip flop 646 to reset the BIR bit 408 to 0. NXSU2 648 and NXSU1 650 represent the next state of the logic controlling the Burst In Range mode. BIR bit 408 is an input to logic 636 so that a reset BIR bit remains reset until a low to high transition on SEQ I/O line 570. Assuming that the drive interface status register 510 has already been cleared of error status bits, the resetting of BIR bit 408 signifies that the Burst In Range mode is now ready to be activated.

The Burst In Range mode is activated when the sequencer determines that the read-write head is within range of the target data sector. When the ASIC learns from the sequencer that the read-write head is within range of the target data sector, SEQIOX 626 and its complement NSEQIOX 628 change to 1 and 0 respectively. As a result, logic 634 changes NCLRBIR 642 from 1 to 0, which in turn causes logic 636 to set BIR 408 to 1. The set BIR bit 408 then triggers logic gates 536-549 in FIG. 47 to permit error status bits 403 to pass from the mask counters 522-528 to the drive interface status register 510. Turning to FIG. 55, BIR bit 408 enters INTERPT block 601. Referring to FIG. 56's illustration of the INTERPT block 601, BIR bit 408 is inverted by inverter 652 and passed to NOR gate 654. NOR gate 654 generates NINHIB signal 656 based on the inverted BIR bit 408 and IFERROR

signal 658. The IFERROR signal 658 is set to 1 if the RO180-RO188 bits indicate that a servo error condition was recorded in the drive interface status register 510. Thus, NINHIB signal 656 is 0 if the BIR bit 408 is 0 or if IFERROR signal 658 indicates an error status bit was set in the drive interface status register 510. A zeroed NINHIB signal 656 goes to NANDs 659 to inhibit error status bits 403 from passing to drive interface status register 510. Therefore, the drive interface status register 510 is updated with new error statuses if and only if the BIR bit 408 is enabled and if the register 510 does not already indicate the existence of an error condition.

FIG. 56 further shows that the servo error status register 500 consists of nine D flip flop circuits 660-668 and the drive interface status register 510 comprises eight D flip flop circuits 670-677. Buses 678 and 680 permit the microprocessor to communicate with the servo error status register 500 and the drive interface status register 510 respectively. The microprocessor uses CLRSTAT signal 682 to clear the servo error status register 500 of error status bits 401 and the CLRDRV signal 684 to clear the drive interface status register 510 of error statuses.

FIG. 57 is the detailed circuitry comprising the mask count register 532 and circuitry to perform miscellaneous functions not immediately related to the masking mechanism. The mask count register 532 is a sixteen-bit register implemented by sixteen D flip flops 690-705 that are loaded by the microprocessor over bus 706 with a counter value corresponding to the error status when an error condition is detected. For each error condition detected, the appropriate two or three bits of the sixteen bits R01A0-R01A15 representing the count value(s) are loaded into one of the mask counters shown on FIG. 58.

FIG. 58 illustrates the mask counters 710-720 of the mask circuit 520. Each mask counter handles one error

condition. When the error condition is detected, a count value is loaded into the mask counter from the applicable bits R01A0-R01A12 of the mask count register 532 (see FIG. 57), and concurrent with each successive servo field 562, the mask counter is decremented by one if the corresponding error status bit 401 is deasserted (i.e., the same error condition has not repeated itself). If the corresponding error status bit 401 is asserted at the successive servo field 562, the mask counter is reloaded with the proper count value. Each time a servo field 562 is detected, the drive interface status register 510 receives error status bits 403 from those mask counters 710-720 that contain non-zero values. After a mask counter has been decremented to zero, it remains at zero until reloaded.

Referring to FIG. 56, once an appropriate servo error condition is detected during the Burst In Range mode, the drive interface status register 510 sends error statuses R0180-R0188 over bus 680 to the safety circuit 574 on FIG. 51. If any of error statuses R0180-R0188 is set to indicate the presence of an error condition, safety circuit 574 inhibits writing to the disk by setting Rd_Wr line 722 high.

FIGs. 52, 53, 55, 59 and 60 illustrate the detailed circuitry used to implement the Special Data Sector mode. In FIG. 52, the sector pulse generator 578 generates a sector mark pulse 580 on SECTOR line 724 for every data sector of interest 564 detected under the read-write head. These sector mark pulses are indirectly used to increment LDSEC register 583.

In FIG. 53, the BRSTNMB register 588 is cleared upon the index mark on a track. When the servo demodulator circuit (not shown) detects a servo field, INCMOD signal 726 is triggered to increment the BRSTNMB register 588. Thus, the BRSTNUM register 588 contains the identifying number of the most recently detected servo field and sends this number out onto BRSTNUM bus 619.

FIG. 54 contains circuitry used to initialize and activate the Special Data Sector mode. Inhibit_sector_pulse_generation bit 582 is set to inhibit sector pulse generation and propagates as NDSECMODE signal 728 to logic 730 which generates signals NCLRALLOW 732 and NSETALLOW1 734. Signals NCLRALLOW 732 and NSETALLOW1 734 go to logic 736 to generate signal ALLOWSECT 738. Signal ALLOWSECT 738 controls whether the sector pulse generator 578 generates sector mark pulses 580. If ALLOWSECT 738 is 0, sector pulse generation is inhibited. Special Data Sector mode bit 581 is set to activate the Special Data Sector mode. Logic 740 controls the sequencing through the Special Data Sector mode.

In FIG. 55, INTERPT block 601 receives error status bits 401 and outputs the contents of the LDSEC register 583 and BDSEC register 584 to the microprocessor.

FIG. 59 illustrates the LDSEC register 583 which contains the number of the most recent data sector since the onset of the Burst In Range mode. The register 583 is initialized by the software prior to engagement of the Burst In Range mode and, after initiation of the Burst In Range mode, loaded with the identifying number of the first target data sector. Load signal LDDSEC 742 causes the identifying number to be loaded from lines LDSEC0-LDSEC7 into the LDSEC register 583. CNTDSEC signal 744 is triggered whenever a data sector is detected and increments the LDSEC register 583 for each data sector that passes under the read-write head. If IFERROR signal 658 indicates that an error condition was sent to the drive interface status register 510, HLDDSEC signal 746 freezes the contents of LDSEC register 583.

FIG. 60 depicts the BDSEC register 584 into which bits from the LDSEC register 583 (i.e., LDSEC0-LDSEC7) are latched whenever a servo field is detected. The detection of a servo field is indicated by a signal on BURST line 748. The BDSEC register 584 contains the number of the most recent data sector at the occurrence of each servo

field 562. In the event of an error condition allowed by the mask circuit 520 as indicated by IFERROR line 658, the BDSEC register 584 is frozen with the number of the last data sector to be detected prior to the error. The contents of the LDSEC and BDSEC registers 583, 584 reveal the exact data sector 564 during which the error condition occurred so that the proper data sectors 564 can be re-accessed.

FIGs. 64A and 64B are software flowcharts showing how the Burst In Range mode and the Special Data Sector mode may be used together in a disk drive. In step 760, the Unsafe Enable Bit 572 is initialized. In step 761, the mask count register 532 is loaded with count values for each type of error condition. In particular, the sixteen-bit mask count register 532 is loaded with two three-bit and five two-bit count values. FIGs. 64A-64B assumes that the disk drive is to read, write or format the "N" data sectors spanning from target data sector number "X" to target data sector number "Y." In order to keep track of how many of the target data sectors have been read/written, the software can either (1) compare the identifying number of the most recently detected data sector with the identifying number of the last target data sector to be read/written, or (2) compare the number of data sectors read/written with the number of target data sectors to be read/written. To implement the first alternative embodiment, the LDSEC register 583 and BDSEC register 584 are initially loaded with "X" which is assumed to be the identifying number of the first target data sector in step 762. To implement the second alternative embodiment, the LDSEC register 583 and BDSEC register 584 are initialized to zero instead. In step 763, the BRSTNMB counter 588 is loaded with "Z" which is assumed to be the identifying number of the first target servo sector. In step 764, the inhibit_sector_pulse generation bit 582 is set to inhibit sector pulse generation. In step 765, the sequencer is told to read,

write or format the N data sectors between data sector number X and data sector number Y. At this time, SEQ I/O line 570 is low because the read/write head is not yet over the target data sectors. In step 766, the inhibit_sector_pulse generation bit 582 is reset to allow sector pulse generation upon servo burst number Z. Further, Special Data Sector mode bit 581 and the Unsafe Enable Bit 572 are activated. At this point, the ASIC is waiting for the SEQ I/O line 570 to go high, indicating that the read/write head has reached the target data sectors. In step 767, the sequencer is searching for the first target data sector X, during which time the SEQ I/O line 570 is low. In step 768, any detected error conditions that occurred prior to reaching the first target data sector X are ignored since the errors pertain to data sectors not of interest. If no errors have been detected so far and the sequencer finds the first target data sector X, the sequencer sets the SEQ I/O line 570 high in step 769 in order to activate the Burst In Range mode and then proceeds to process the target data sectors. Detected error conditions that pass through mask circuit 520 are reported to the drive interface status register 510. In step 770, the sequencer stops processing data sectors if an error condition is detected in the drive interface status register 510, or if the sequencer has finished processing all N target data sectors. At this point, the software must determine how many of the N data sectors were in fact processed without error. In step 771, the software skips the Burst In Range mode if the BIR bit 408 was not set. If the BIR bit 408 was set, the software checks to see if any errors were reported to the drive interface status register 510 (step 772). A zero value in the drive interface status register 510 indicates that unmasked errors were not detected. If no errors were detected, the software checks the BDSEC register 584 to see if all of the N target data sectors were processed (step 773). If not, the process loops back to step 772

until either errors are reported in the drive interface status register 510, or all N target data sectors were processed without error. In step 772, if an error was reported to the drive interface status register 510, the BDSEC register 584 is checked to see if the error(s) relate to a data sector detected after the last target data sector Y of interest (step 774). Errors relating to target data sectors cause the software to proceed to step 775, where the LDSEC register 583 reveals the exact data sector during which the error(s) were detected. The software then returns to step 760. Thus, the Burst In Range mode and Special Data Sector mode can operate singly or in combination.

While the invention is susceptible to various modifications and alternative forms, specific examples thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that it is not intended to limit the invention to the particular forms disclosed, but on the contrary, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following claims.

Claims

1. A removable cartridge for a disk drive having a spindle motor, said removable cartridge comprising:

a cartridge housing;

a disk contained within said cartridge housing and having a disk hub for mounting to the spindle motor of the disk drive;

a cartridge hub having a camming surface;

a camming structure having a cam which engages the camming surface of said cartridge hub to move said camming structure between a first position and a second position, where said camming structure in the first position presses the disk hub against said cartridge housing so as to prevent rattling of said disk and said camming structure in the second position does not press the disk hub against said cartridge housing; and

a cartridge door movably mounted to said cartridge housing and coupled to said cartridge hub so that movement of said cartridge door between a closed position and an open position rotates said cartridge hub;

wherein movement of said cartridge door from the closed position to the open position rotates said cartridge hub so that the cam of said camming structure moves along the camming surface of said cartridge hub, thereby causing said camming structure to move from the first position to the second position.

2. The removable cartridge of claim 1, wherein rotational movement of said cartridge hub causes vertical movement of said camming structure from the first position to the second position.

3. The removable cartridge of claim 1 wherein

said cartridge housing has a top, a bottom and two side walls;

said cartridge door slides along an arcuate path from one side wall toward the other side wall of said cartridge housing.

4. The removable cartridge of claim 1 wherein said disk is a multi-platter disk.

5. A removable cartridge disk drive system comprising a disk drive and a removable cartridge for insertion into and ejection out of said disk drive wherein

said removable cartridge including:

a disk contained within said cartridge housing and having a disk hub;

a cartridge hub having a camming surface;

a camming structure having a cam which cooperates with the camming surface of said cartridge hub to move said camming structure between a first position and a second position, where said camming structure in the first position presses the disk hub against said cartridge housing so as to prevent rattling of said disk and said camming structure in the second position does not press the disk hub against said cartridge housing; and

a cartridge door movably mounted to said cartridge housing and coupled to said cartridge hub so that movement of said cartridge door between a closed position and an open position rotates said cartridge hub;

said disk drive including:

a spindle motor; and

a door opening mechanism which engages said cartridge door during insertion of said removable cartridge into said disk drive to open said cartridge door, thereby rotating said cartridge hub so that the cam of said camming structure cooperates with the camming surface of said cartridge hub in order to

move said camming structure from the first position to the second position.

6. The removable cartridge disk drive system of claim 5 wherein ejection of said removable cartridge out of said disk drive causes said door opening mechanism to close said cartridge door, thereby rotating said cartridge hub so that the cam of said camming structure cooperates with the camming surface of said cartridge hub in order to move said camming structure from the second position to the first position.

7. The removable cartridge disk drive system of claim 5 wherein

said cartridge door has a catch; and

said door opening mechanism is mounted to said disk drive housing and has an end which engages the catch of said cartridge door so that the insertion of said removable cartridge into said disk drive causes the end of said door opening mechanism to engage the catch of said cartridge door and to pull said cartridge door from the closed position to the open position.

8. The removable cartridge disk drive system of claim 7 wherein said door opening mechanism is pivotally mounted to said disk drive housing so that insertion of said removable cartridge into said disk drive pivots said door opening mechanism in order to engage the catch of said cartridge door and to pull said cartridge door from the closed position to the open position.

9. A removable cartridge for a disk drive having a spindle motor, said removable cartridge comprising:

a cartridge housing having a top, a bottom and two side walls;

an anti-rotation member extending downwardly from the top of said cartridge housing;

a disk contained within said cartridge housing and having a disk hub for mounting to the spindle motor of the disk drive;

a cartridge hub having a camming ramp surface and rotatably movable between a rattle position and an anti-rattle position;

a camming structure comprising:

a recess which cooperates with said anti-rotation member to prevent rotation of said camming structure relative to said cartridge housing;

a bevelled surface; and

at least one camming member which rides along the camming ramp surface of said cartridge hub to move said camming structure between a rattle position and an anti-rattle position, where said bevelled surface of said camming surface in the rattle position presses the disk hub against said cartridge housing so as to prevent rattling of said disk and said bevelled surface of said camming structure in the anti-rattle position does not press the disk hub against said cartridge housing;

a spring coupled between said cartridge hub and said cartridge housing to bias said cartridge hub to the anti-rattle position; and

a cartridge door pivotally mounted to said cartridge housing and affixed to said cartridge hub;

wherein pivoting of said cartridge door from the closed position to the open position rotates said cartridge hub from the anti-rattle position to the rattle position, thereby storing biasing force on said spring and moving the camming member of said camming structure along the camming surface of said cartridge hub in order to move said camming structure from the rattle position to the anti-rattle position.

10. A removable cartridge disk drive system comprising a disk drive and a removable cartridge for insertion into the disk drive, wherein

said removable cartridge including:

a cartridge housing having a top and a bottom;

an anti-rotation member extending downwardly from the top of said cartridge housing;

a disk contained within said cartridge housing and having a disk hub;

a cartridge hub having a camming ramp surface, said cartridge hub rotatably movable between a rattle position and an anti-rattle position;

a camming structure comprising:

a recess which cooperates with said anti-rotation member to prevent rotation of said camming structure relative to said cartridge housing;

a bevelled surface; and

at least one camming member which rides along the camming ramp surface of said cartridge hub to move said camming structure between a rattle position and an anti-rattle position, where said bevelled surface of said camming surface in the rattle position presses the disk hub against said cartridge housing so as to prevent rattling of said disk and said bevelled surface of said camming structure in the anti-rattle position does not press the disk hub against said cartridge housing;

a spring coupled between said cartridge hub and said cartridge housing to bias said cartridge hub to the anti-rattle position; and

a cartridge door pivotally mounted to said cartridge housing and affixed to said cartridge hub;

said disk drive including:

a spindle motor; and

a door opening mechanism which engages said cartridge door during insertion of said removable cartridge into said disk drive;

wherein insertion of said removable cartridge into said disk drive causes said door opening mechanism to pivot said cartridge door from the closed position to the open position, thereby storing biasing force on said spring and rotating said cartridge hub from the anti-rattle position to the rattle position so that said camming member of said camming structure cooperates with the camming surface of said cartridge hub in order to move said camming structure from the anti-rattle position to the rattle position.

11. The method of releasing an anti-rattle feature in a removable cartridge for a disk drive, the removable cartridge including a disk, a cartridge door and an anti-rattle structure which prevents the disk from rattling, the method comprising the steps of:

(a) inserting the removable cartridge into the disk drive;

(b) opening the door of the removable cartridge during the insertion of the removable cartridge; and

(c) using the movement of the door to release the anti-rattle structure in the removable cartridge so that the disk may rattle.

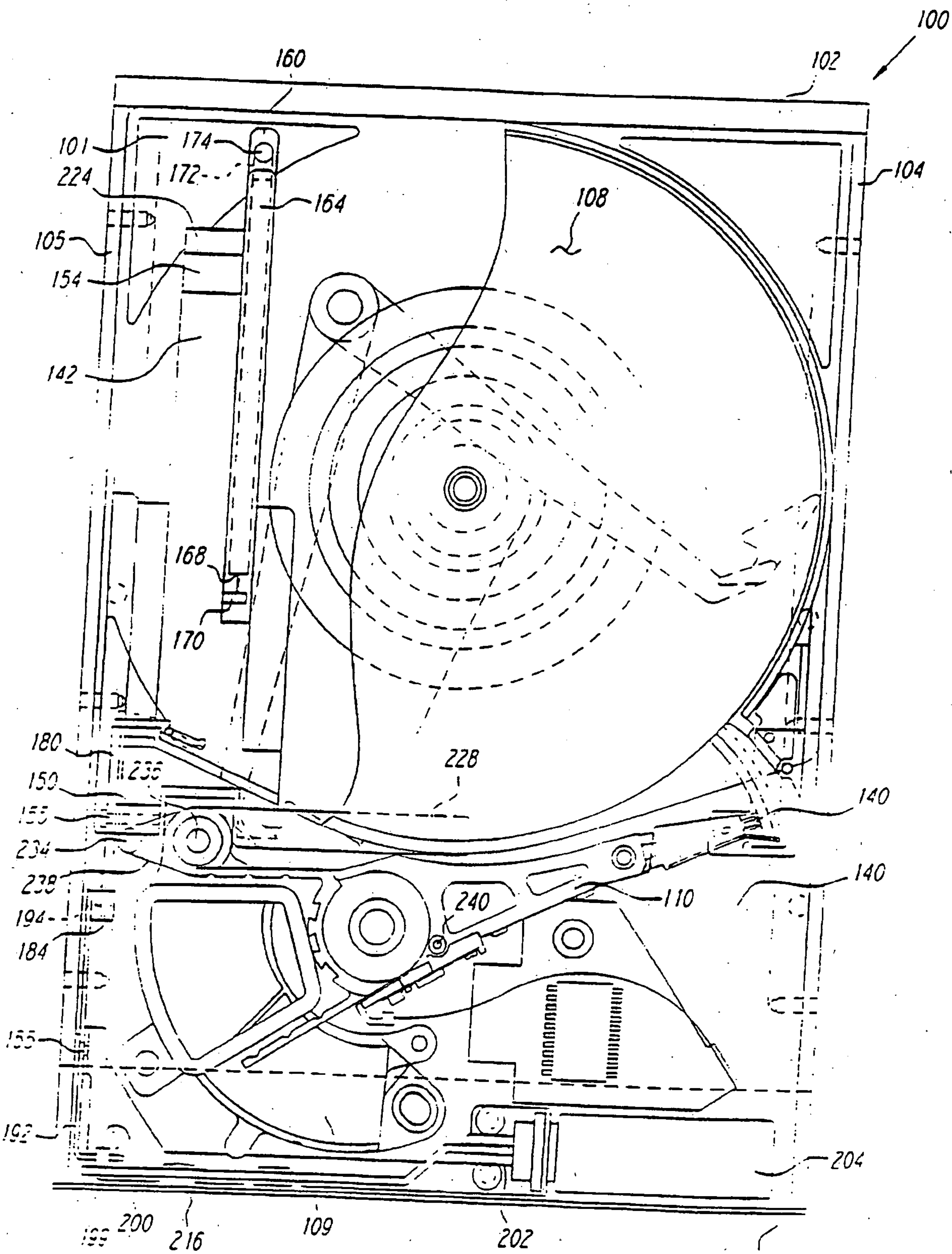
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FIG. 1

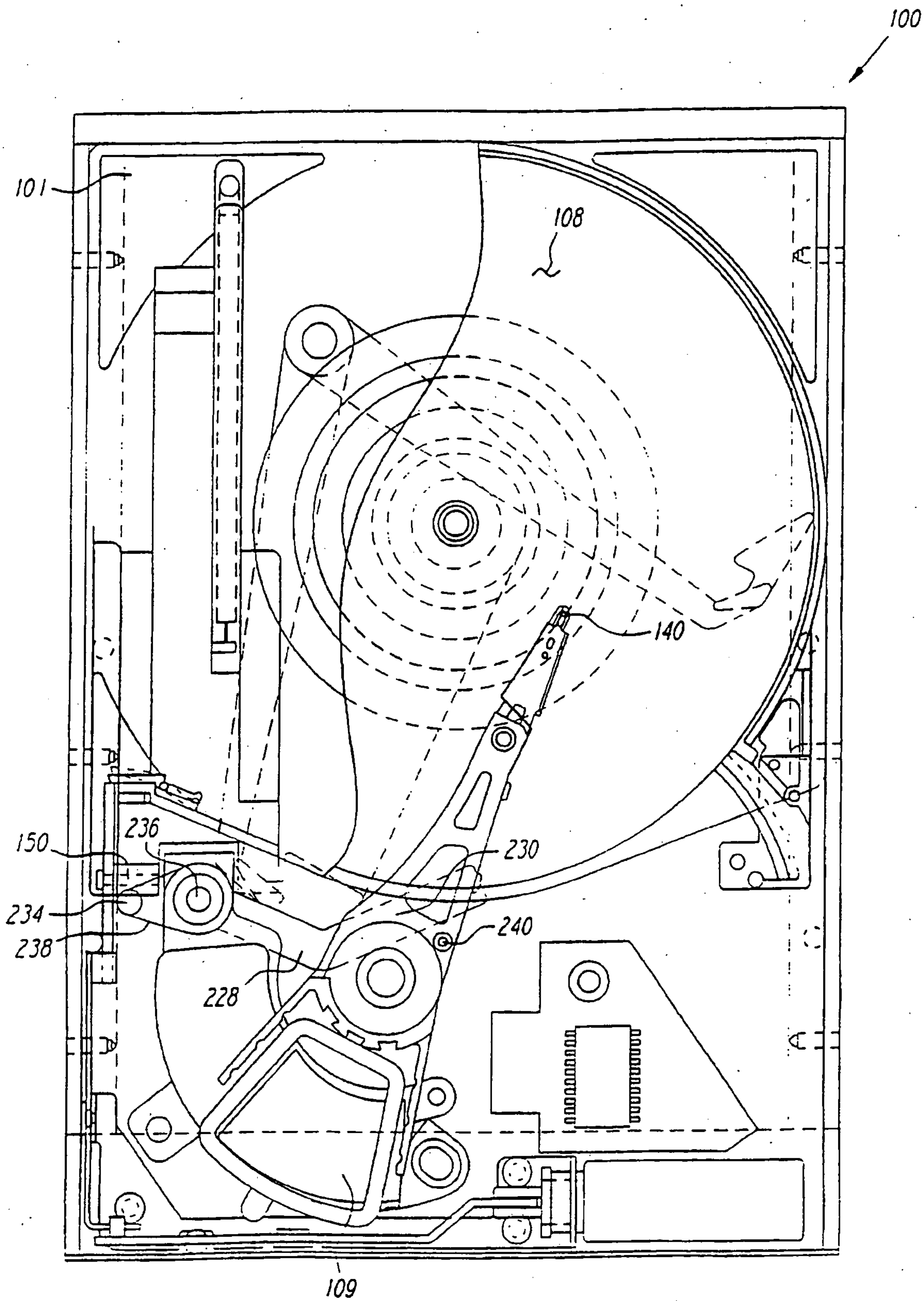


FIG. 2

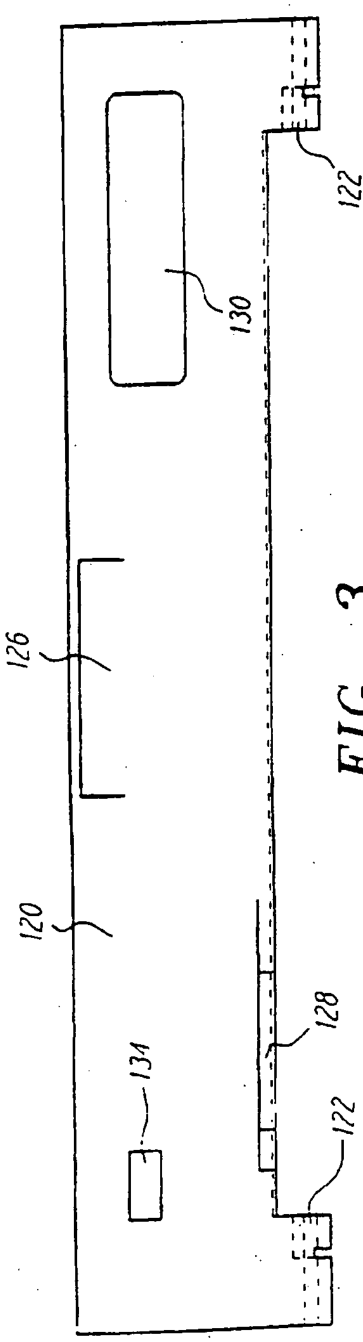


FIG. 3

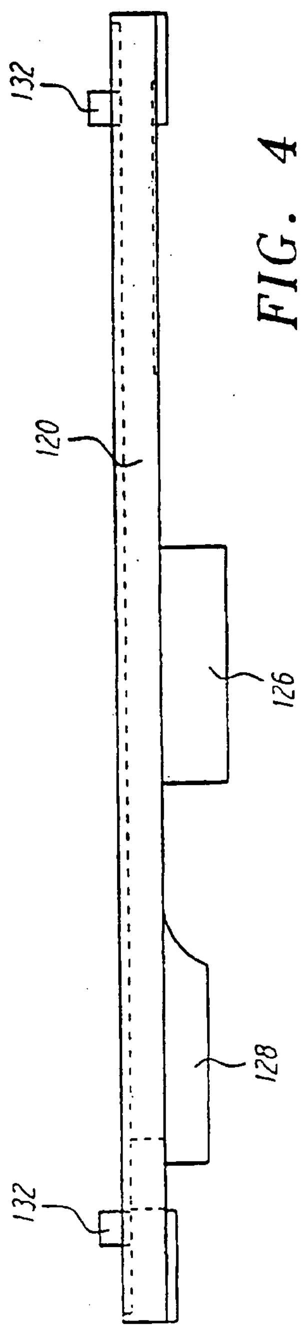


FIG. 4

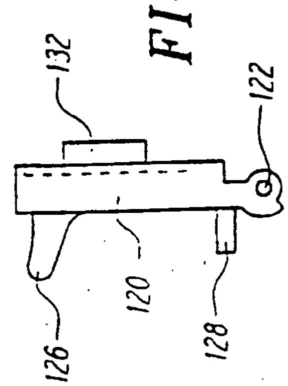


FIG. 5

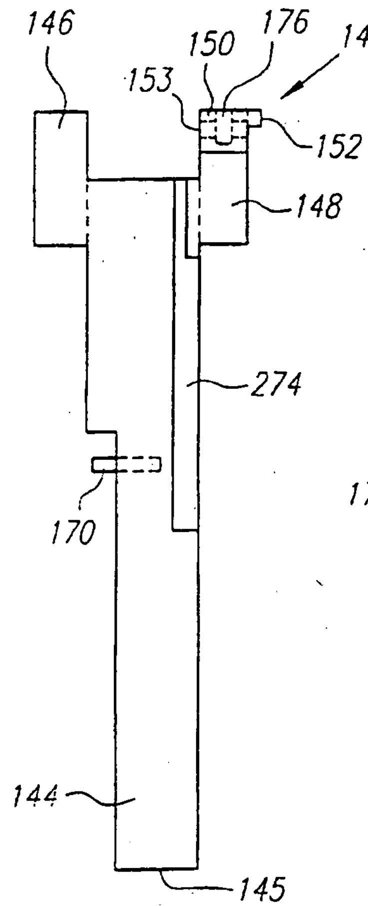


FIG. 6

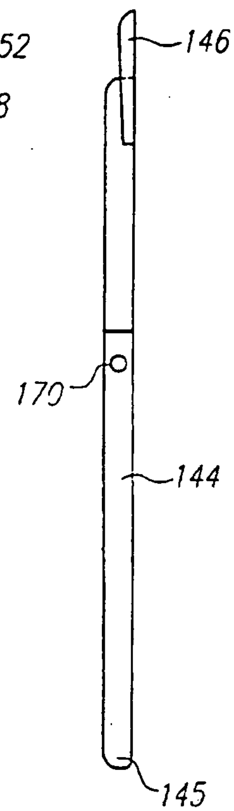


FIG. 7

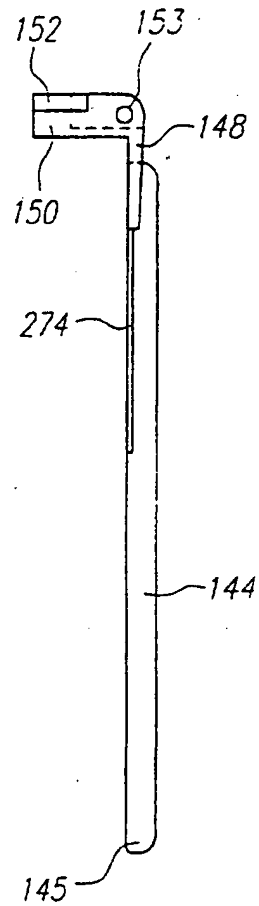


FIG. 8

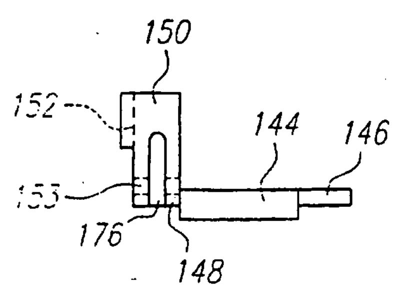


FIG. 9

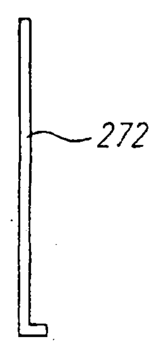


FIG. 33

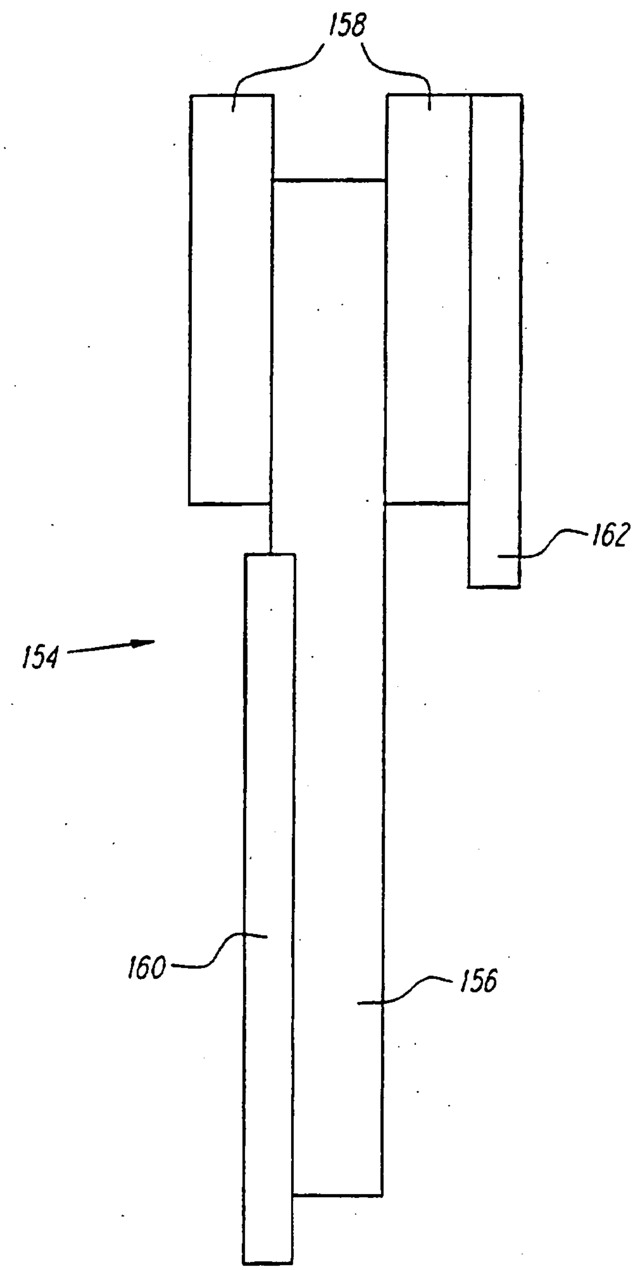


FIG. 10

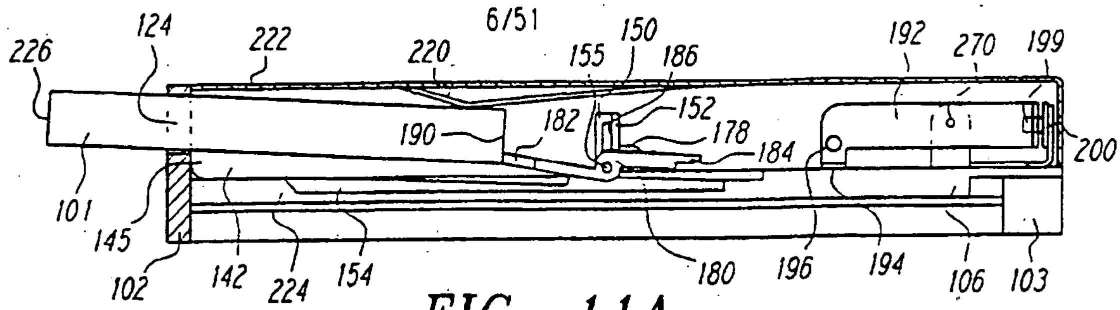


FIG. 11A

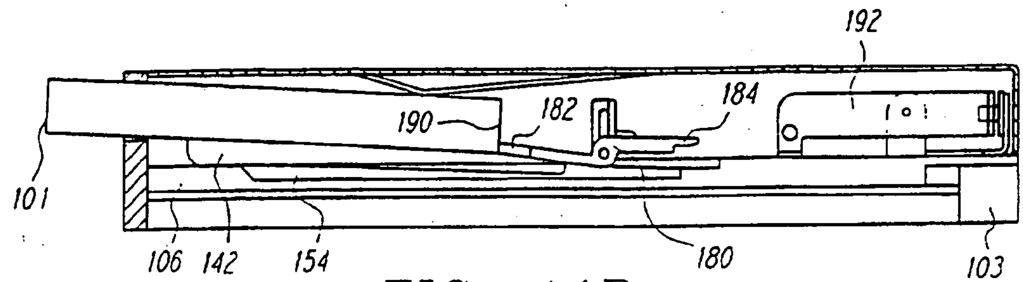


FIG. 11B

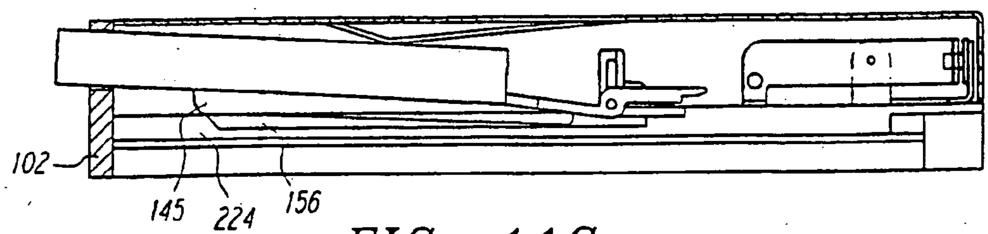


FIG. 11C

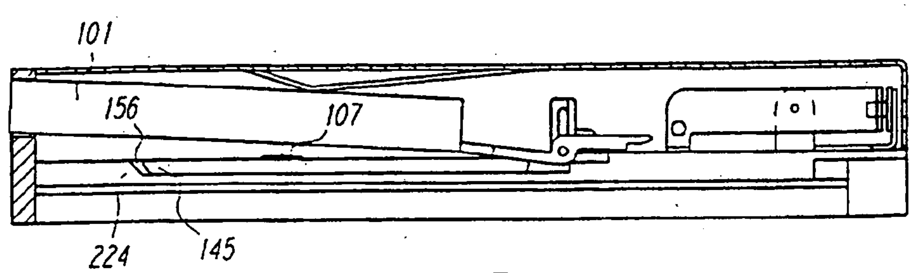


FIG. 11D

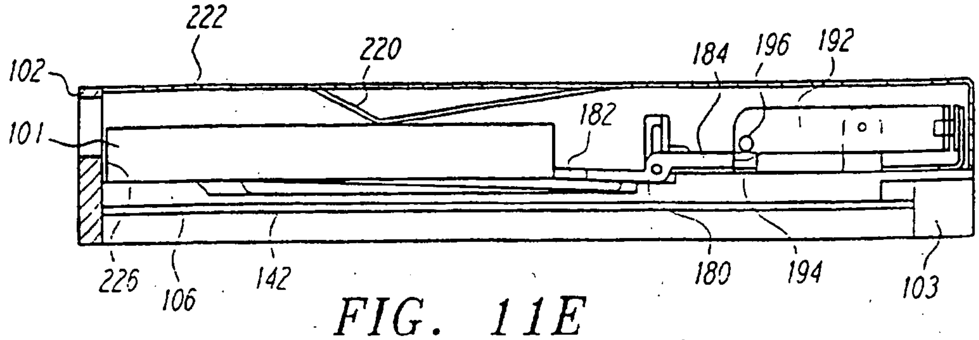


FIG. 11E

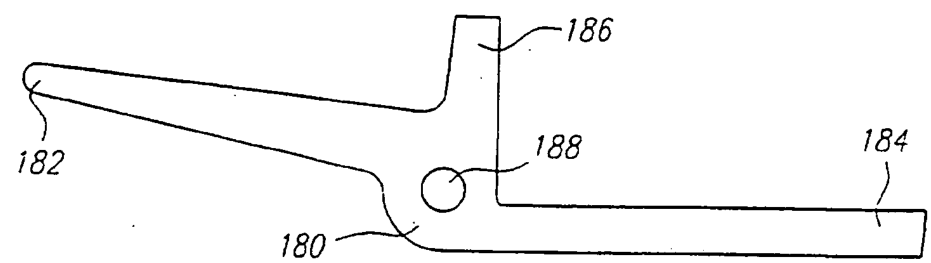


FIG. 12

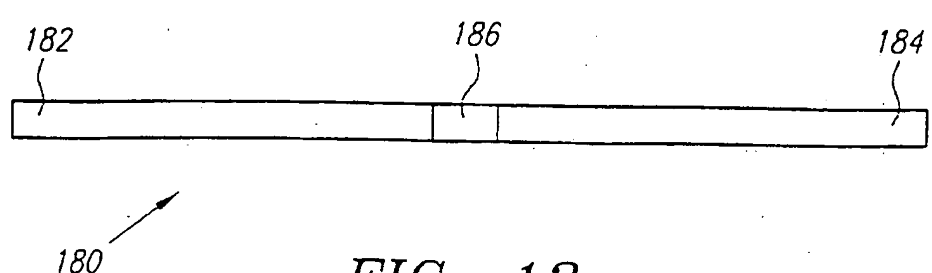


FIG. 13

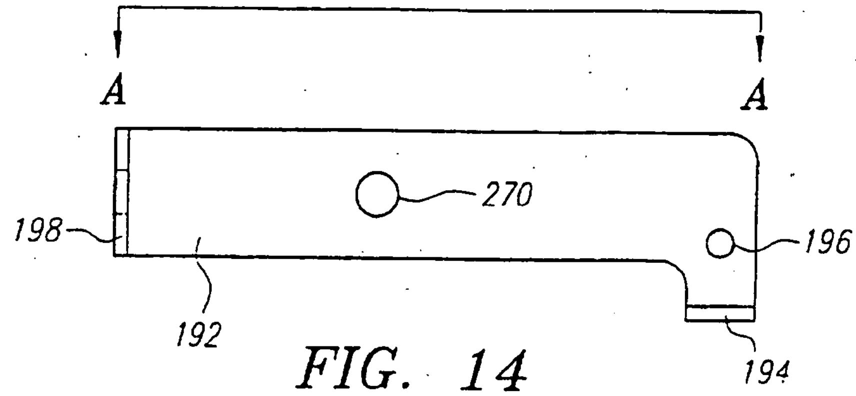


FIG. 14

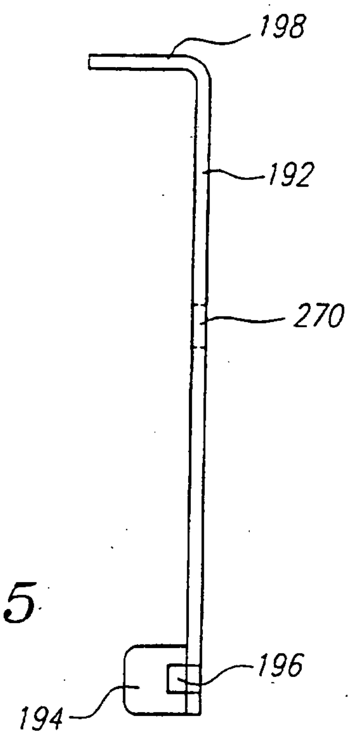
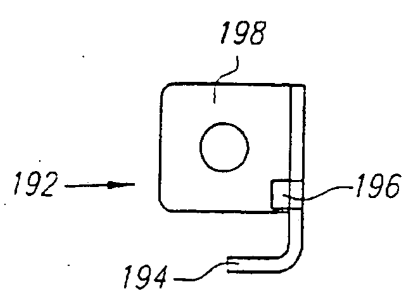


FIG. 15



FIG, 16

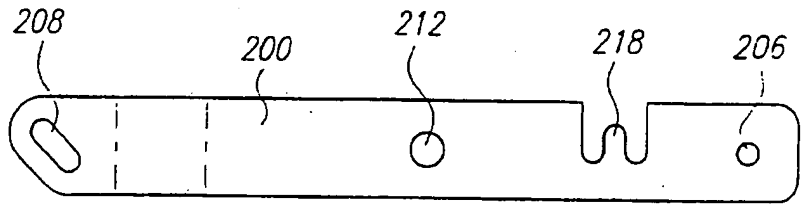


FIG. 17

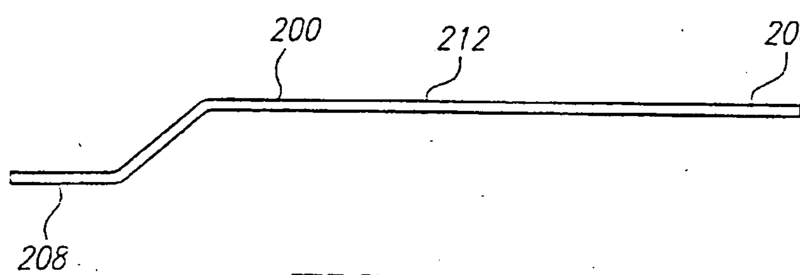


FIG. 18

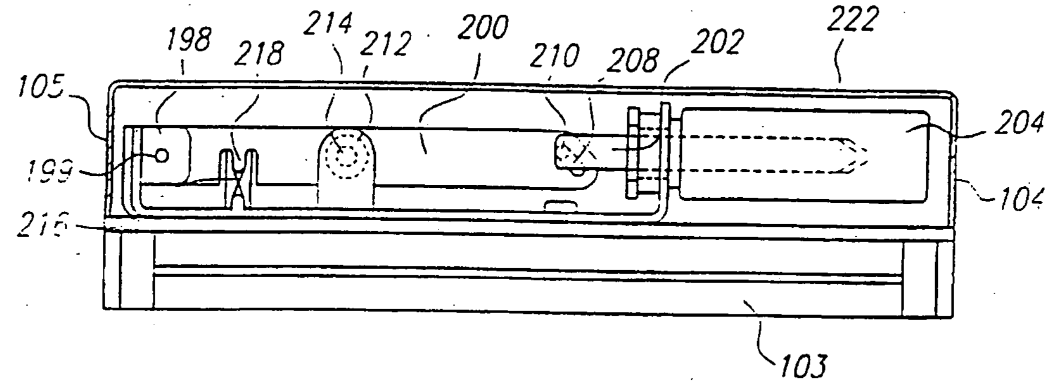

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FIG. 19

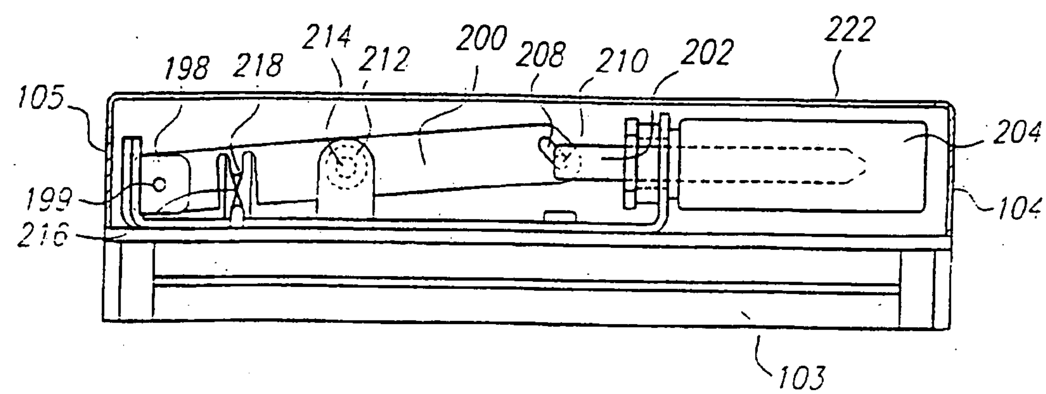
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FIG. 20

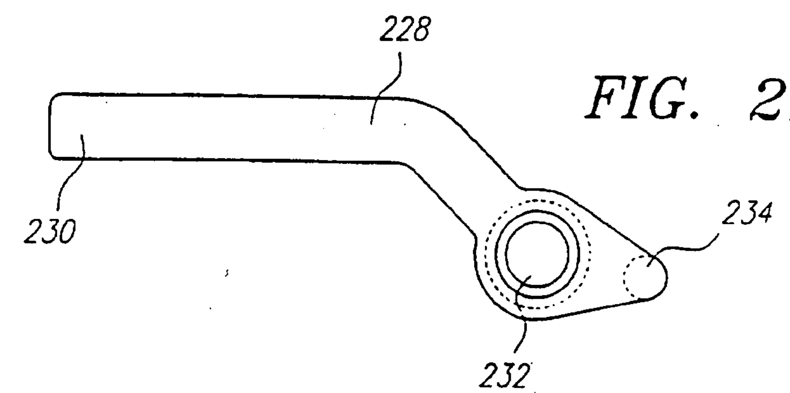


FIG. 21

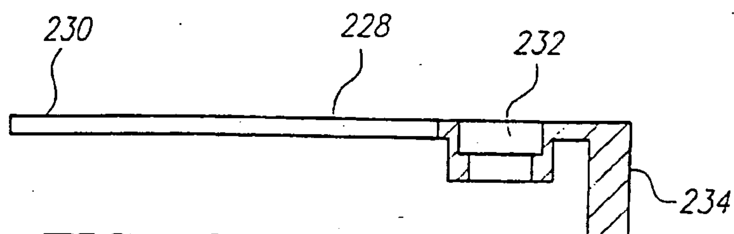


FIG. 22

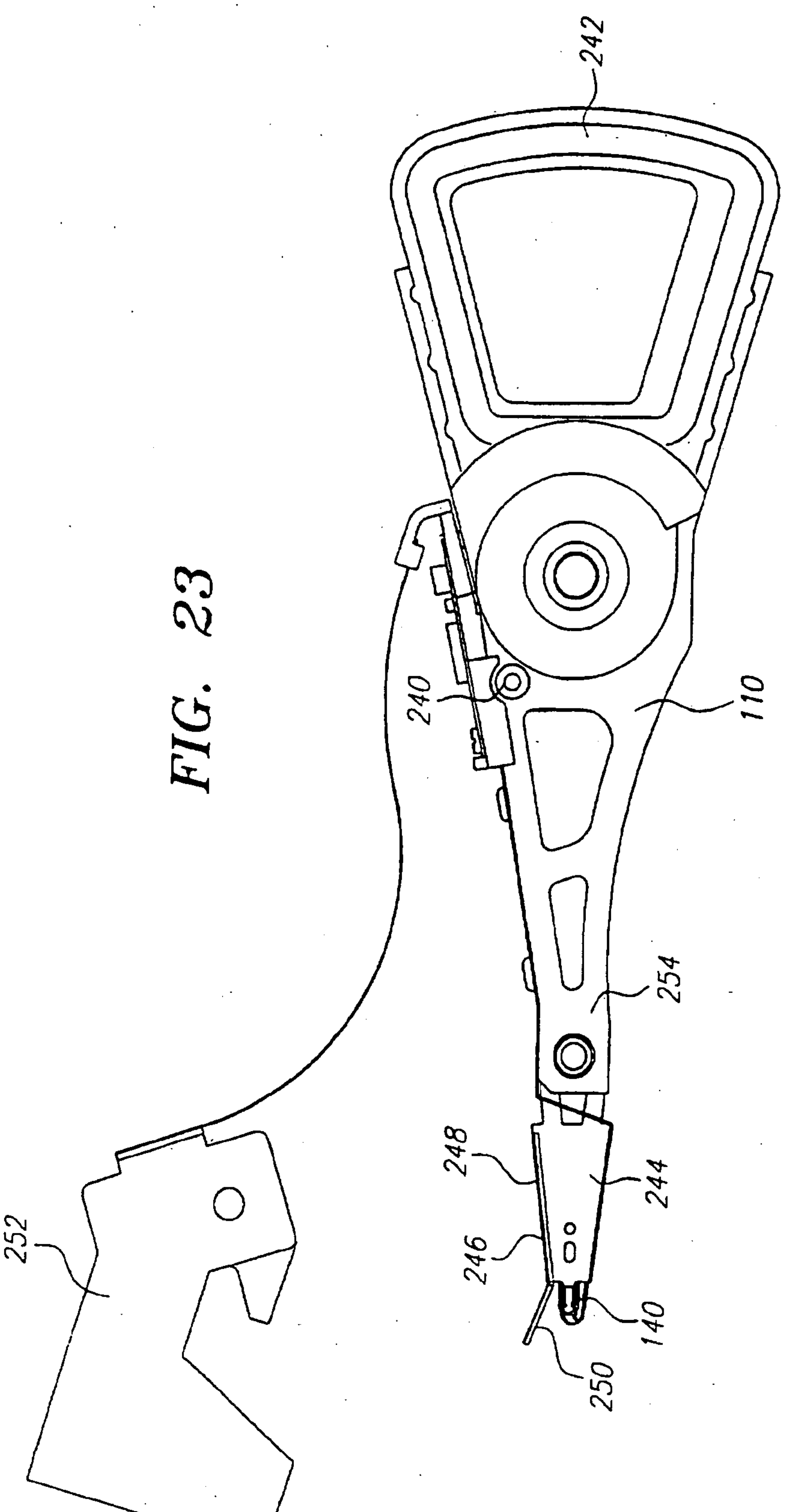


FIG. 23

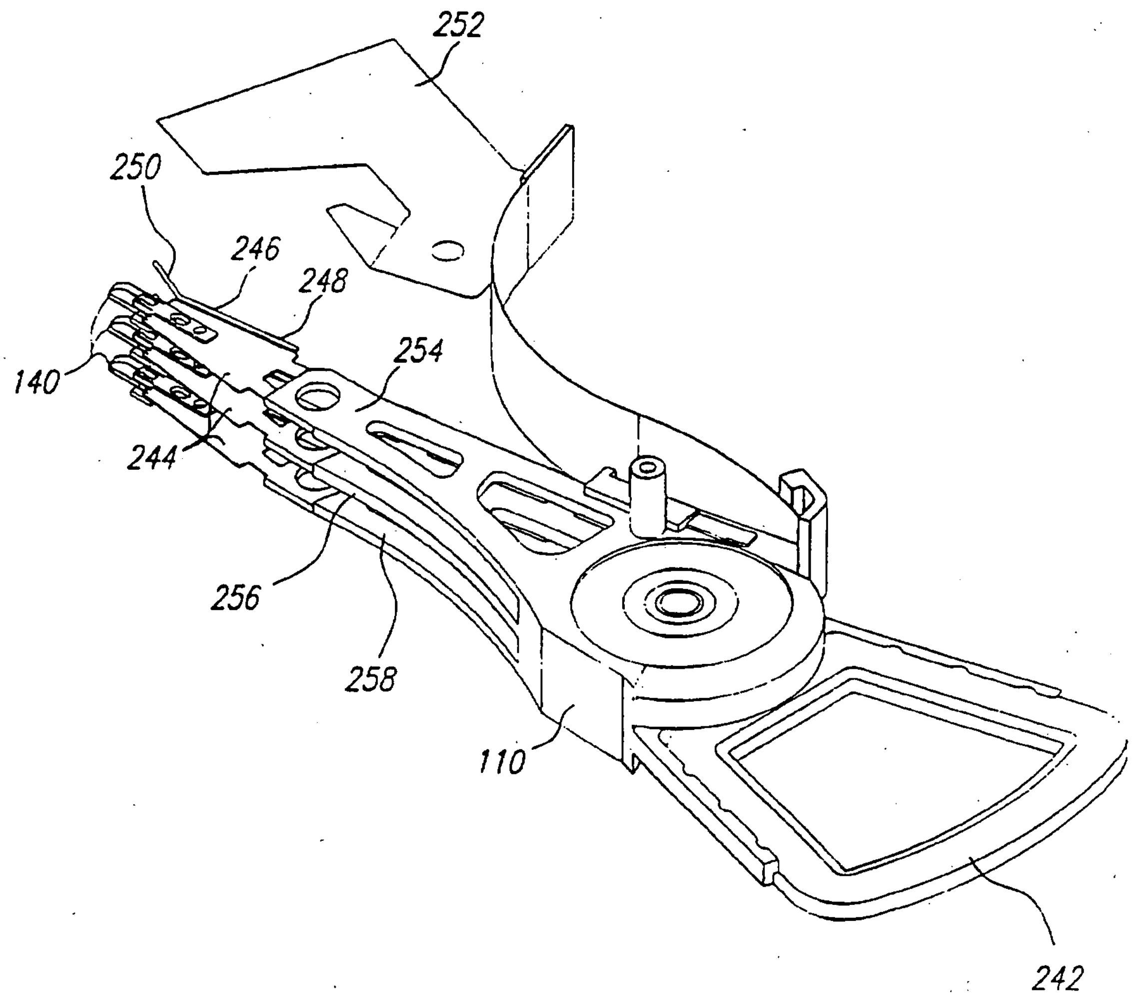


FIG.24

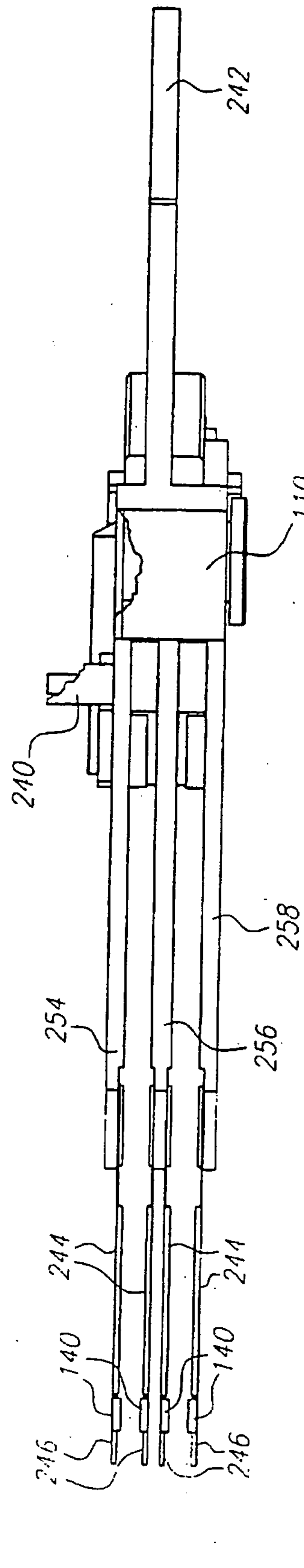


FIG. 25

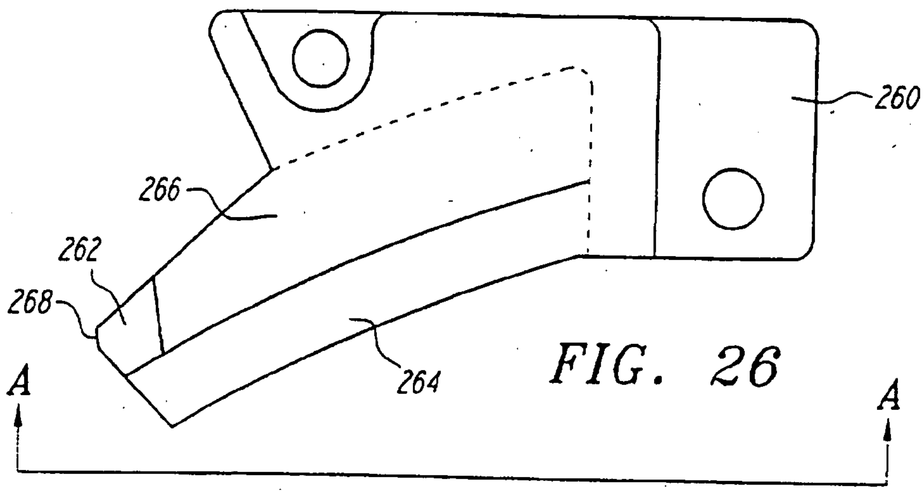


FIG. 26

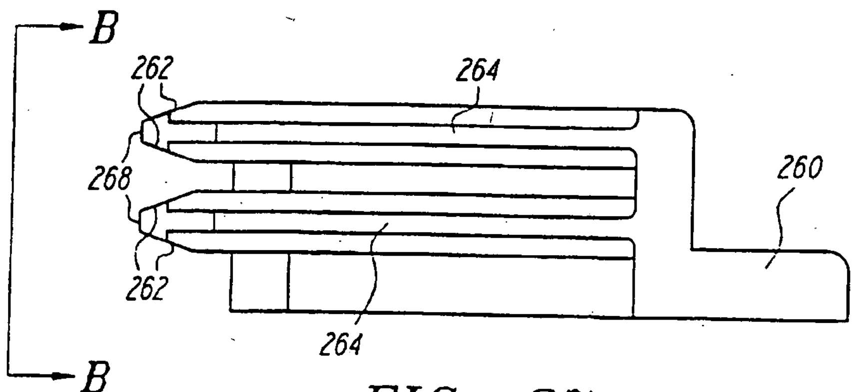


FIG. 27

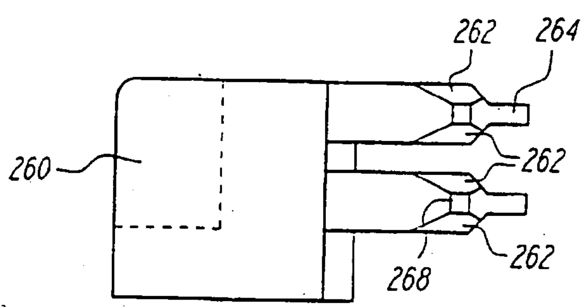


FIG. 28

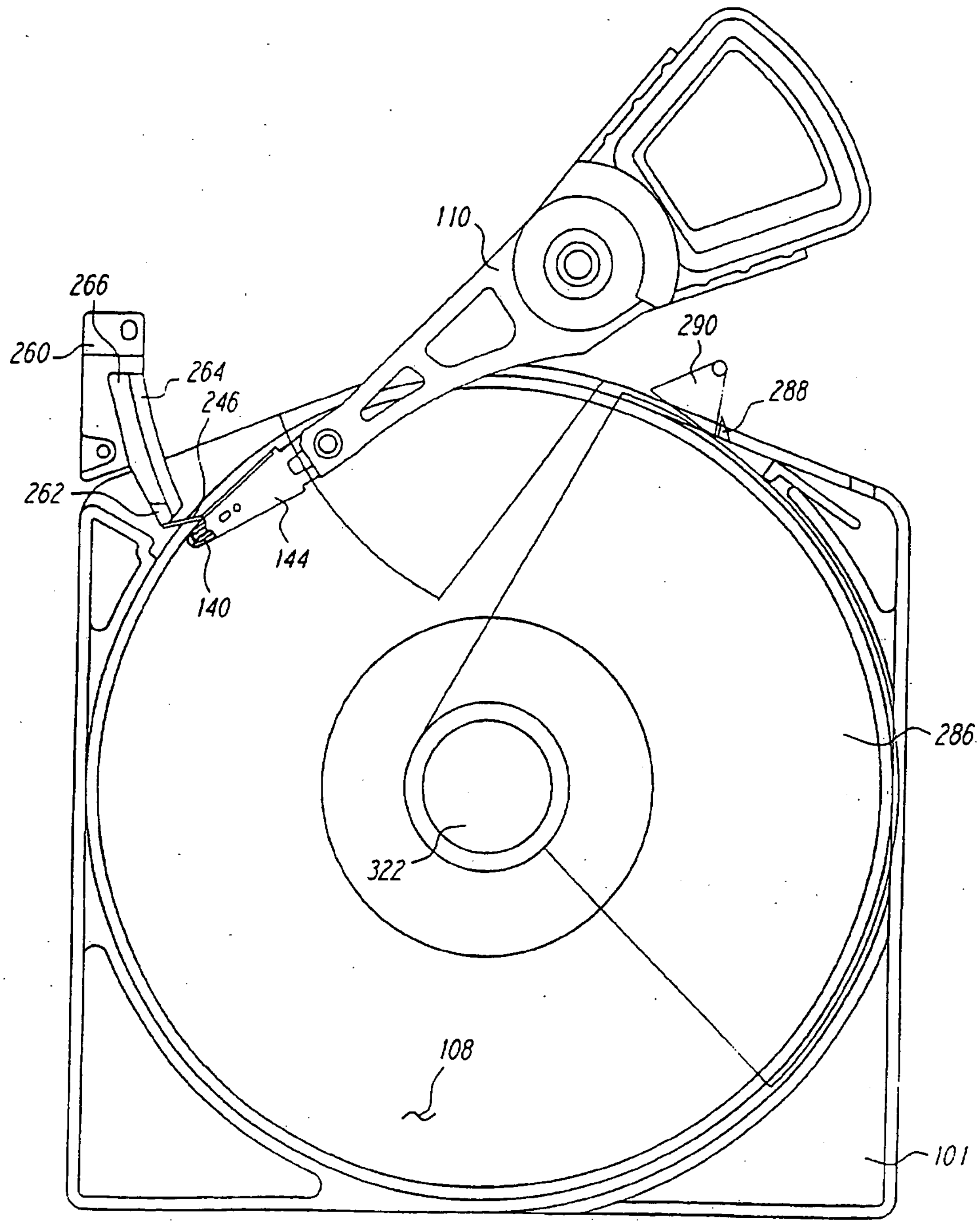


FIG. 29

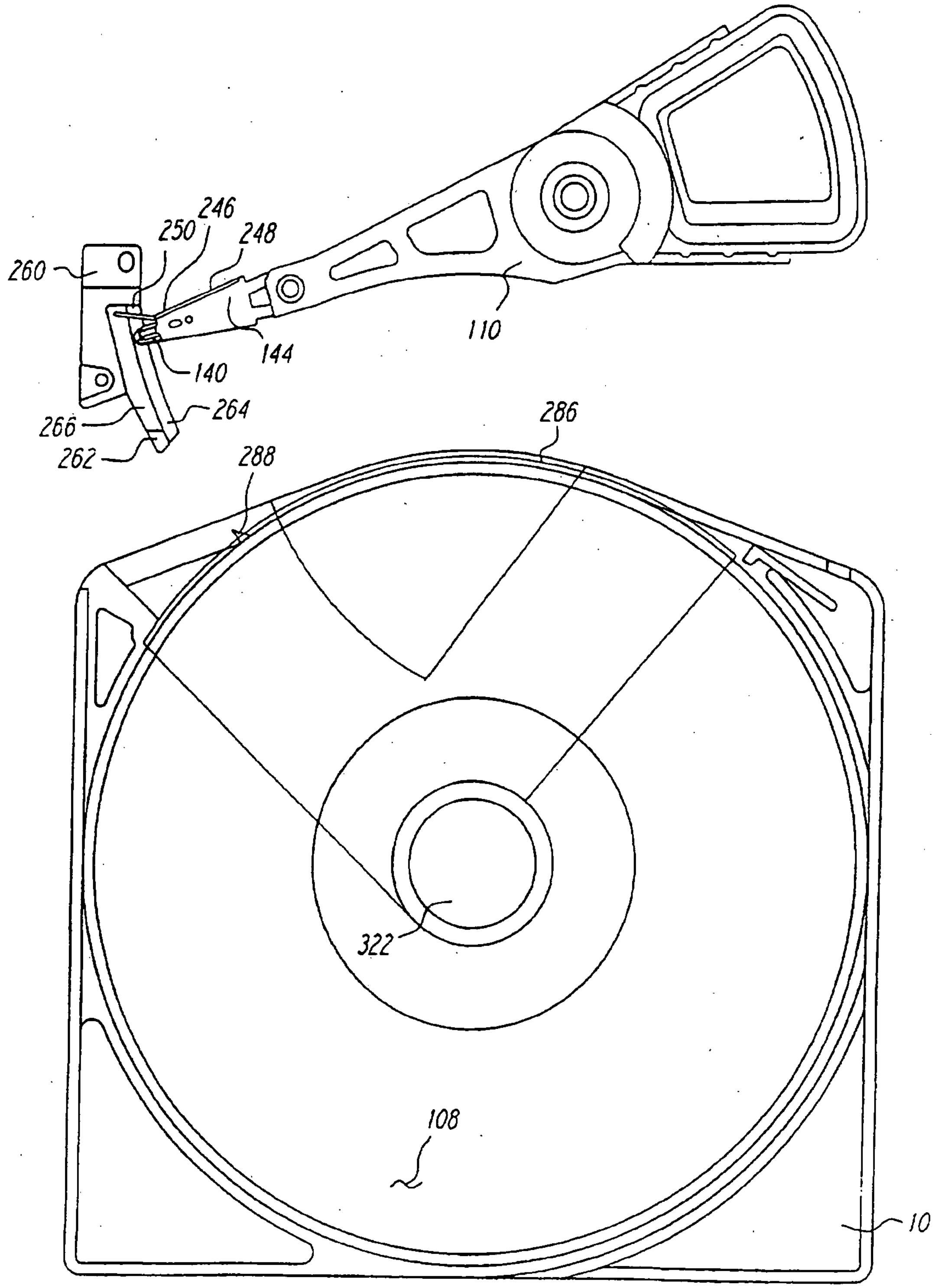
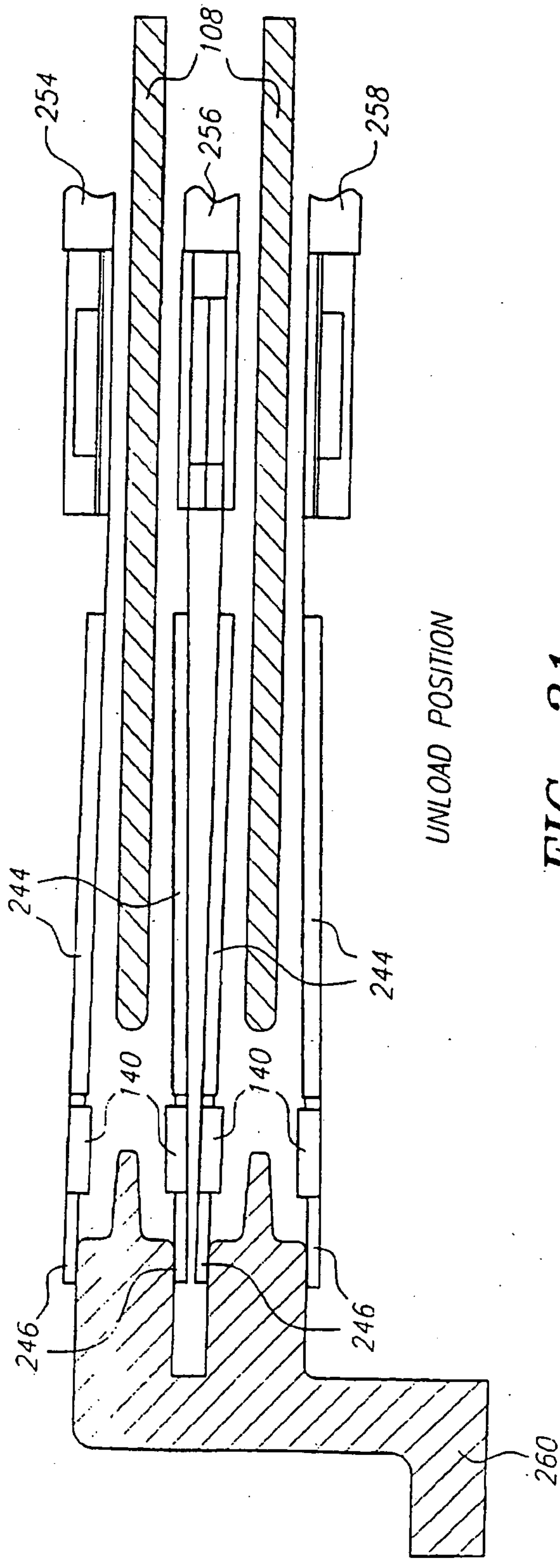
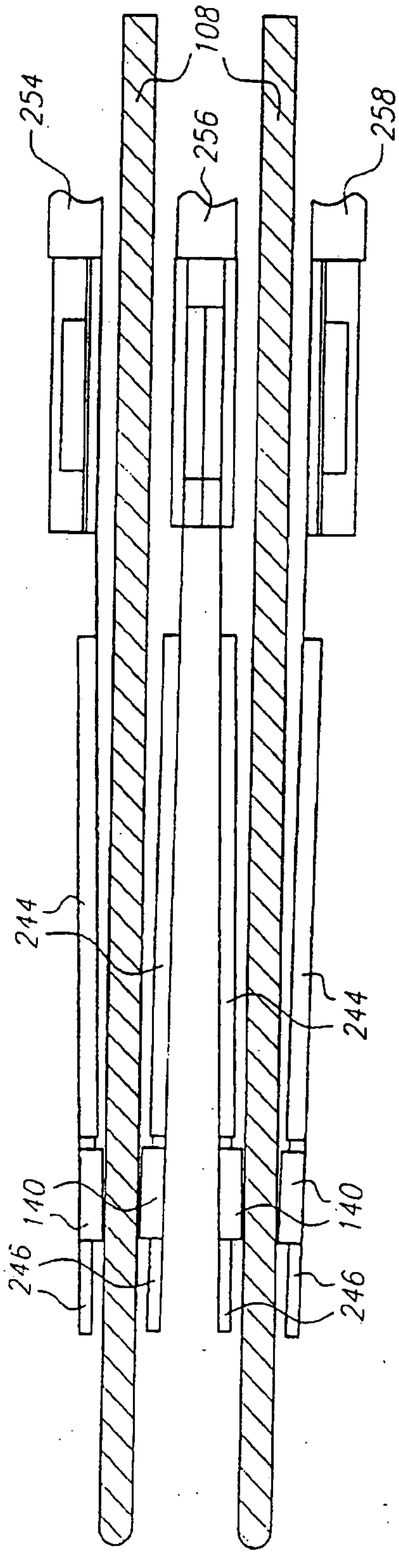


FIG. 30



UNLOAD POSITION

FIG. 31



LOAD POSITION

FIG. 32

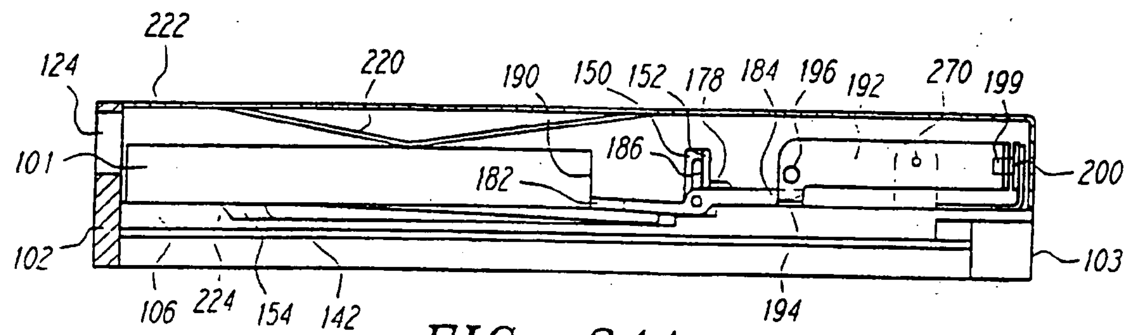


FIG. 34A

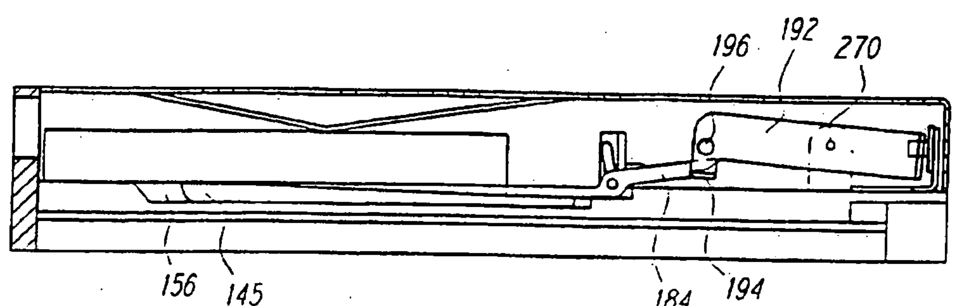


FIG. 34B

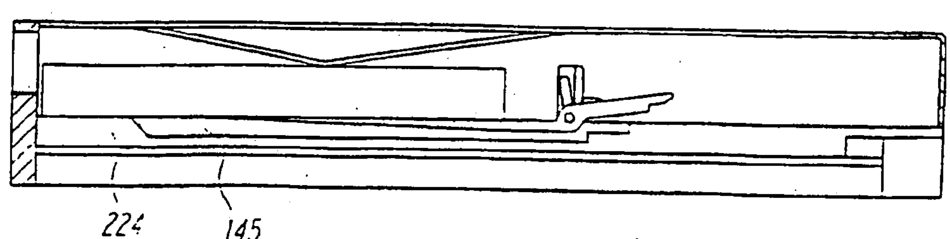


FIG. 34C

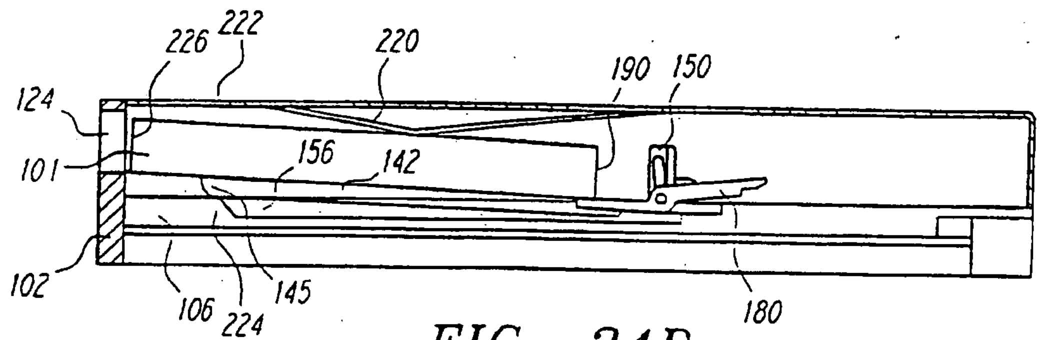


FIG. 34D

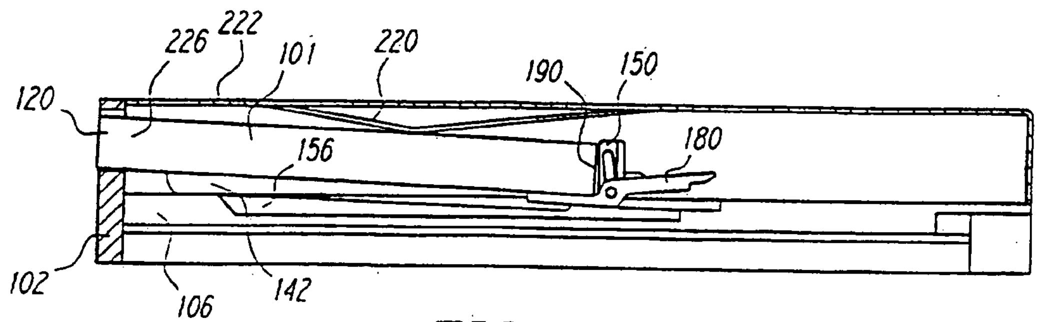


FIG. 34E

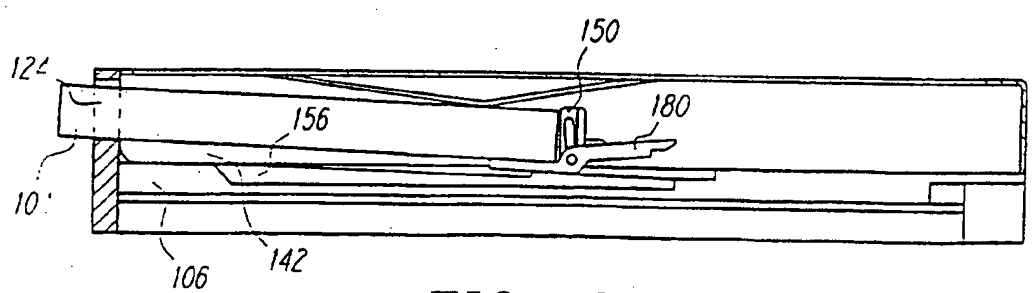


FIG. 34F

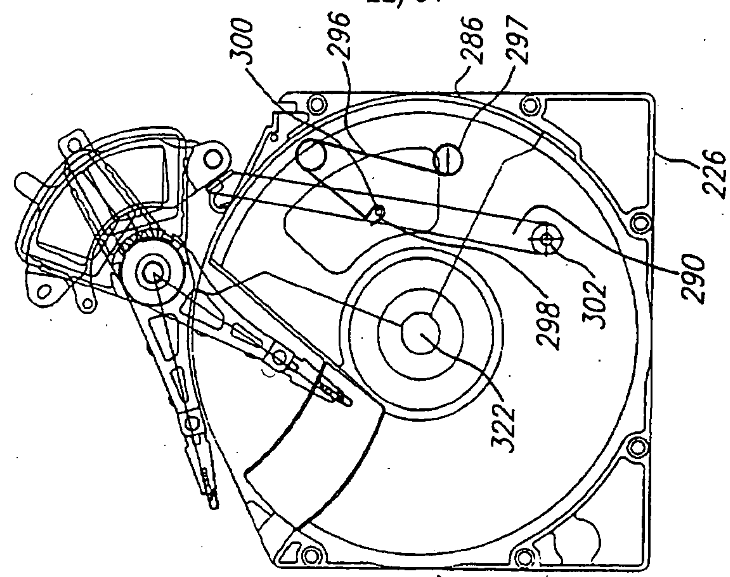


FIG.37

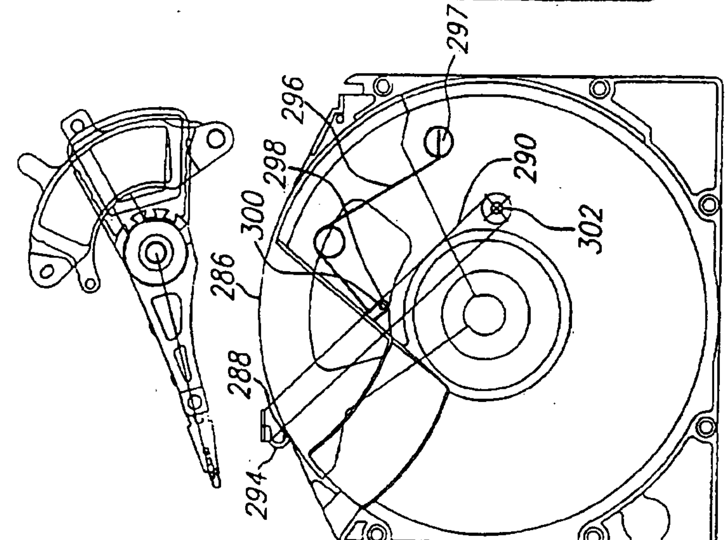


FIG.36

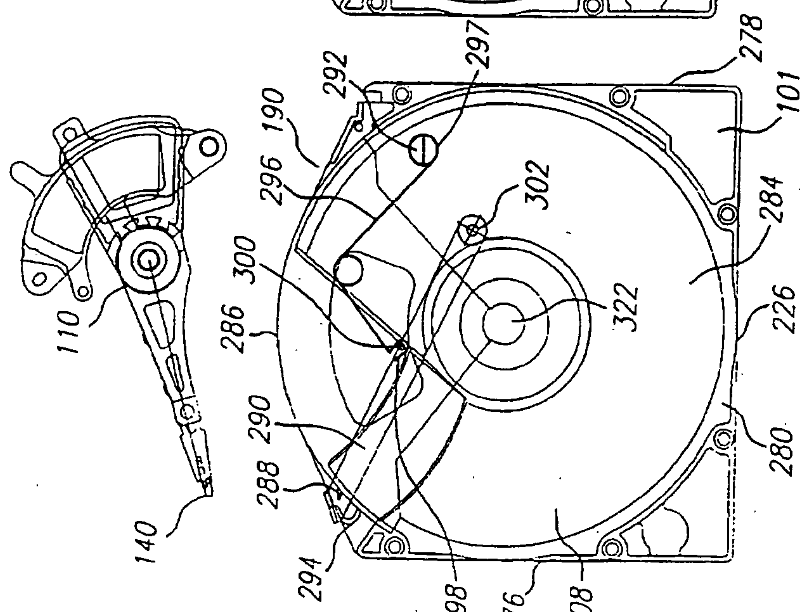


FIG.35

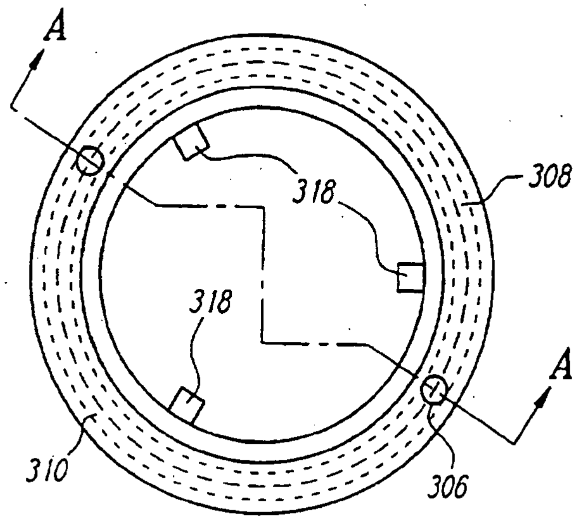


FIG. 38

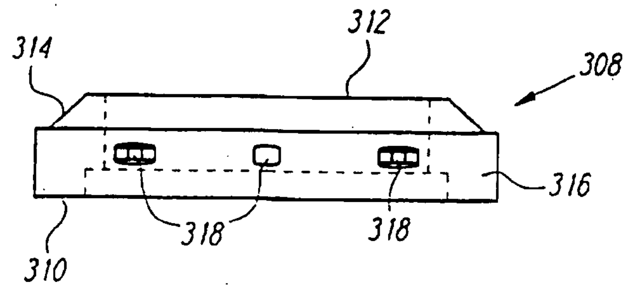


FIG. 39

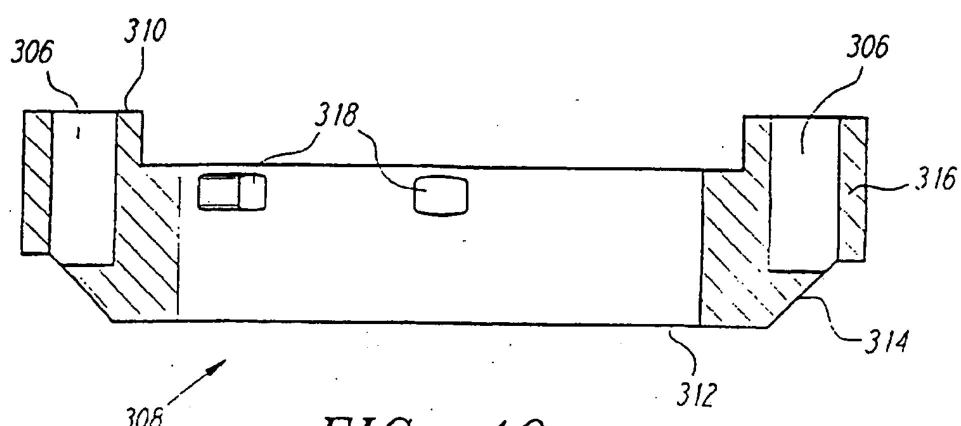


FIG. 40

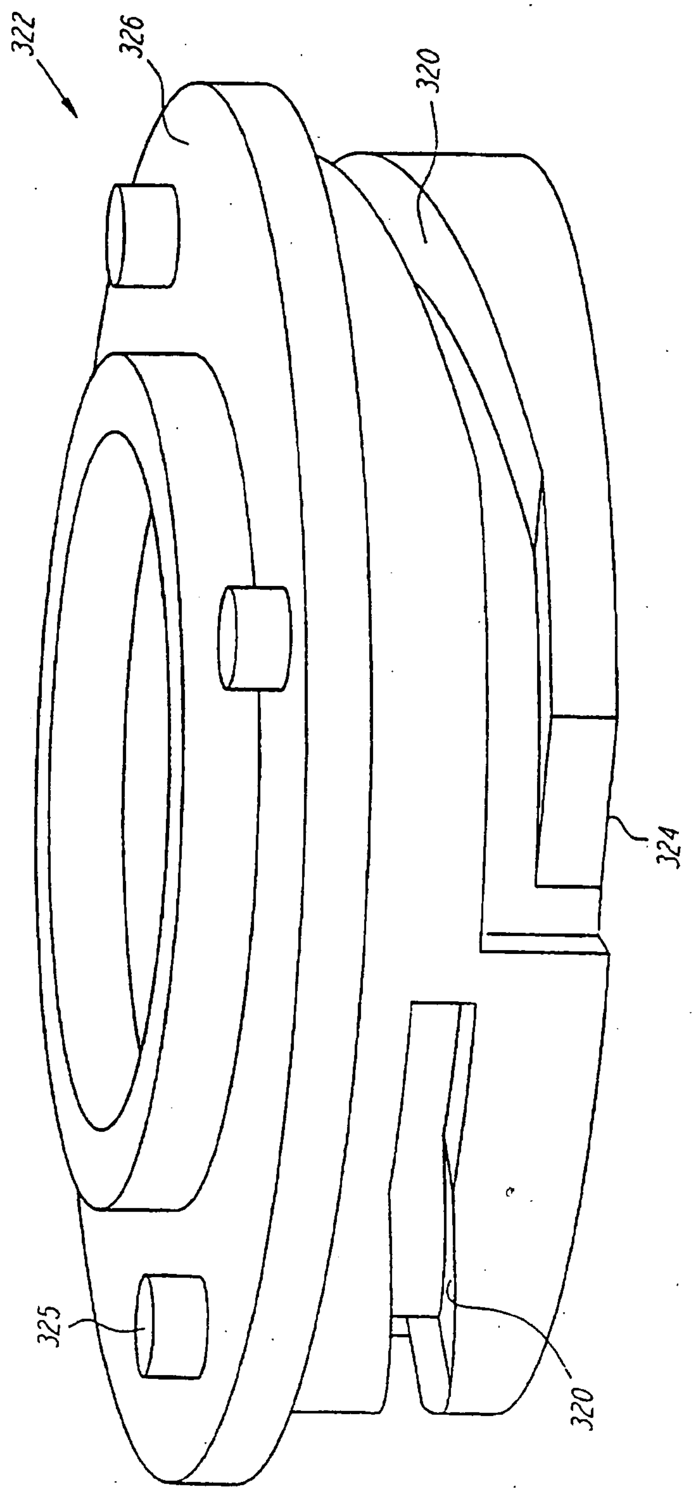


FIG. 41

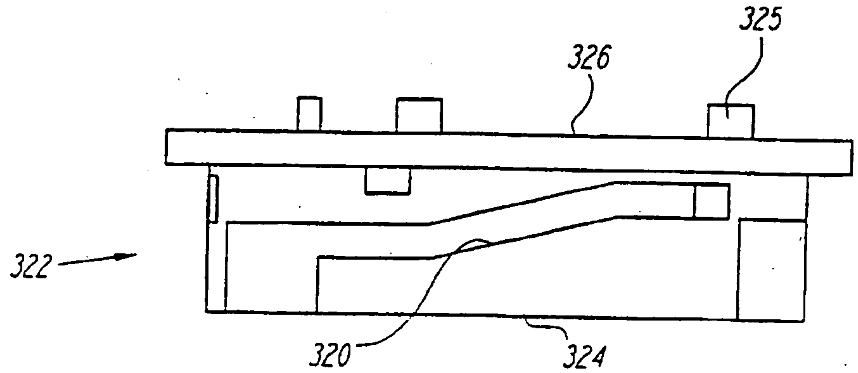


FIG. 42

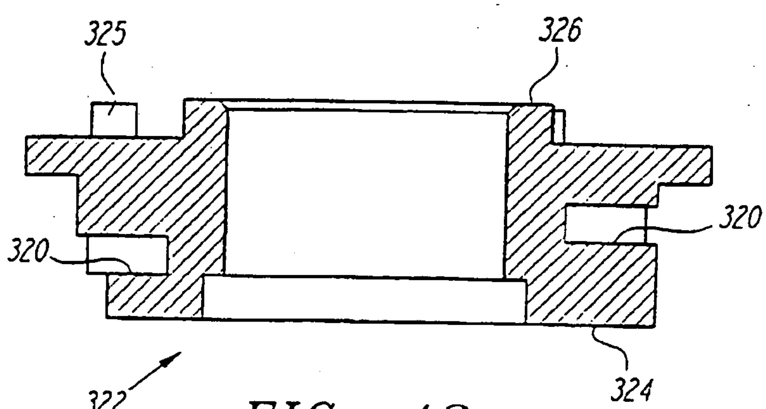


FIG. 43

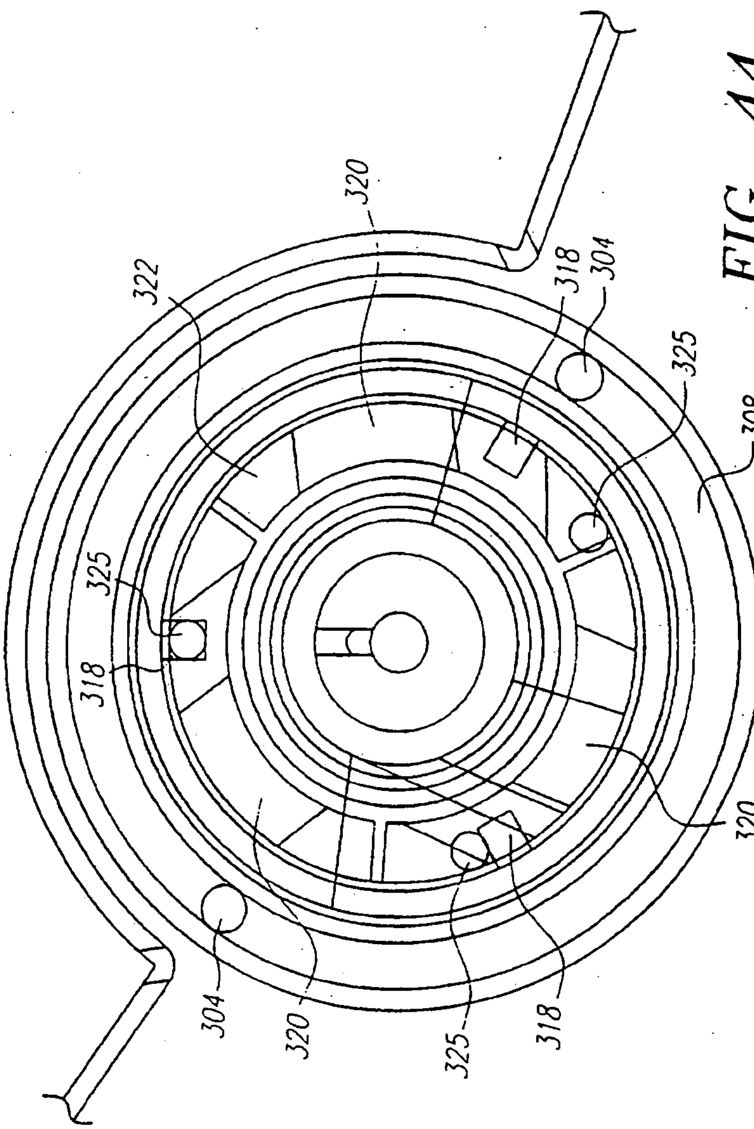


FIG. 44

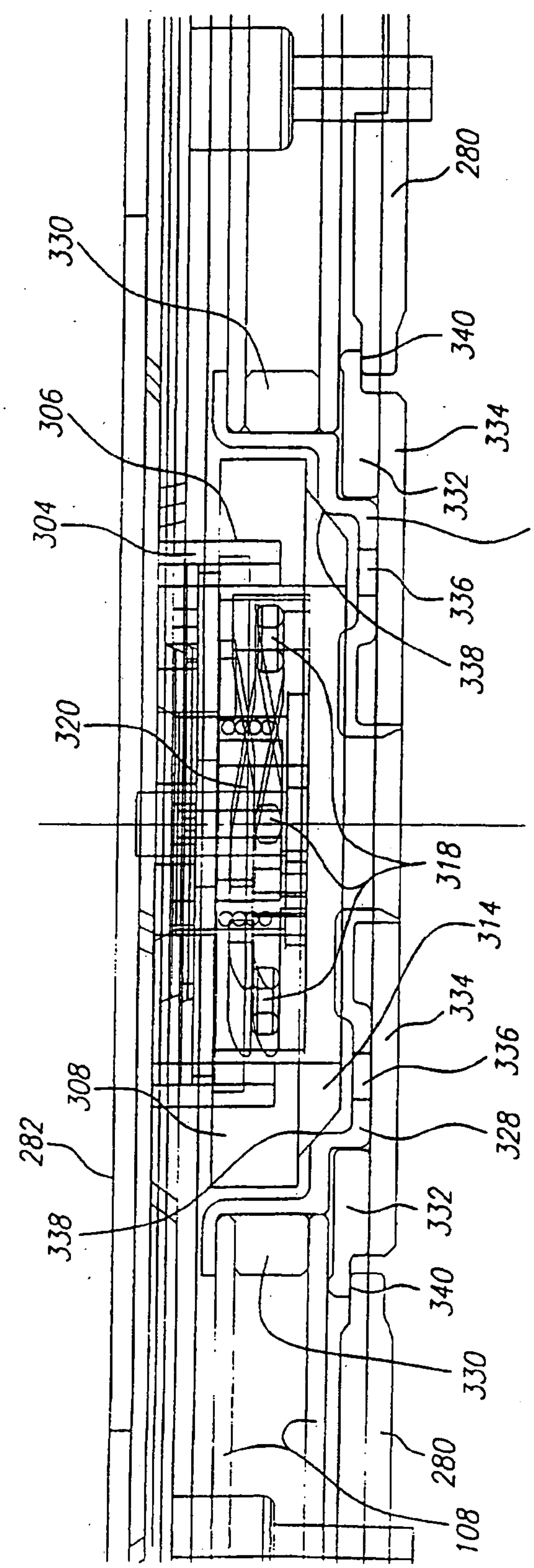


FIG. 45

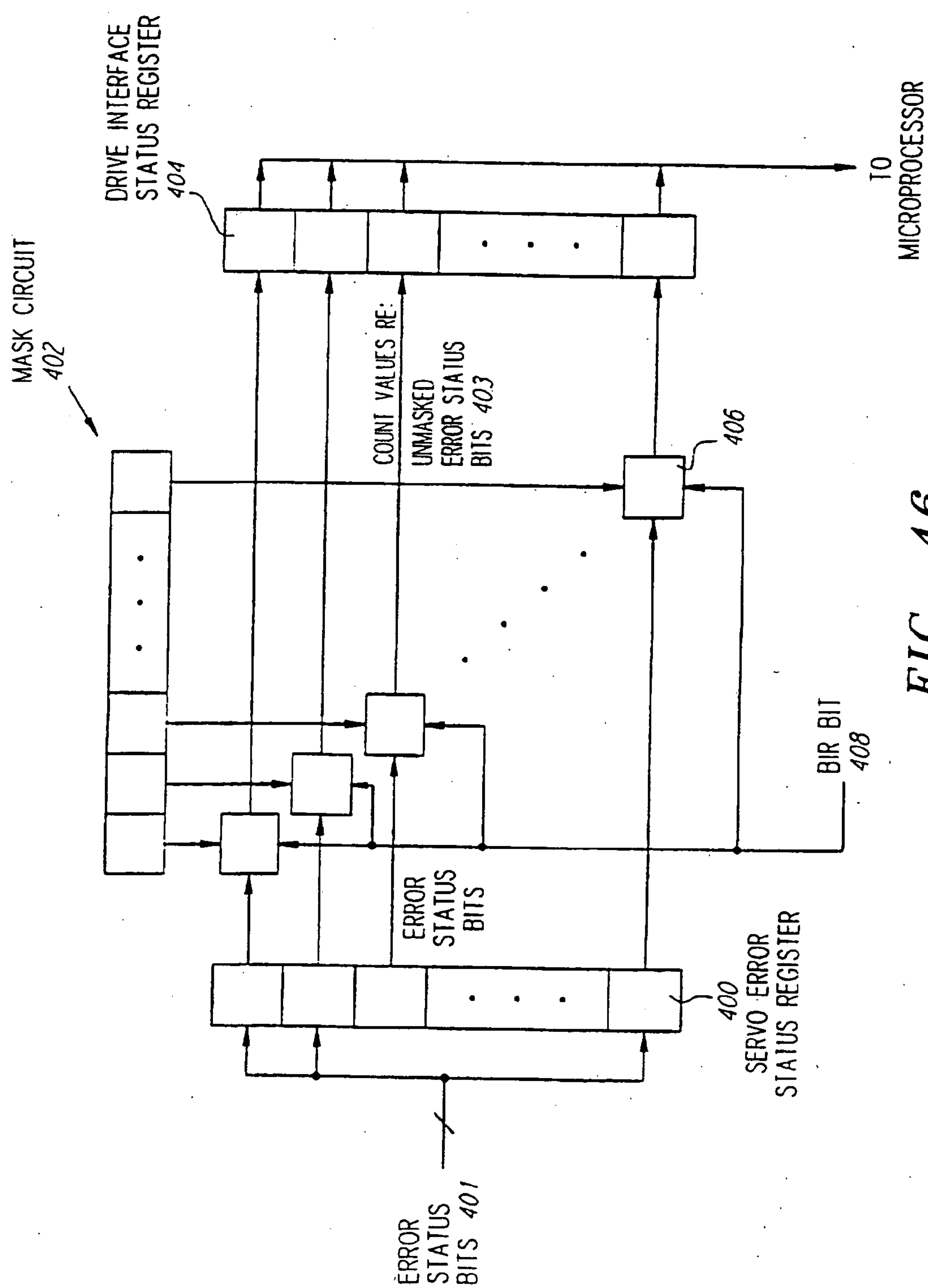
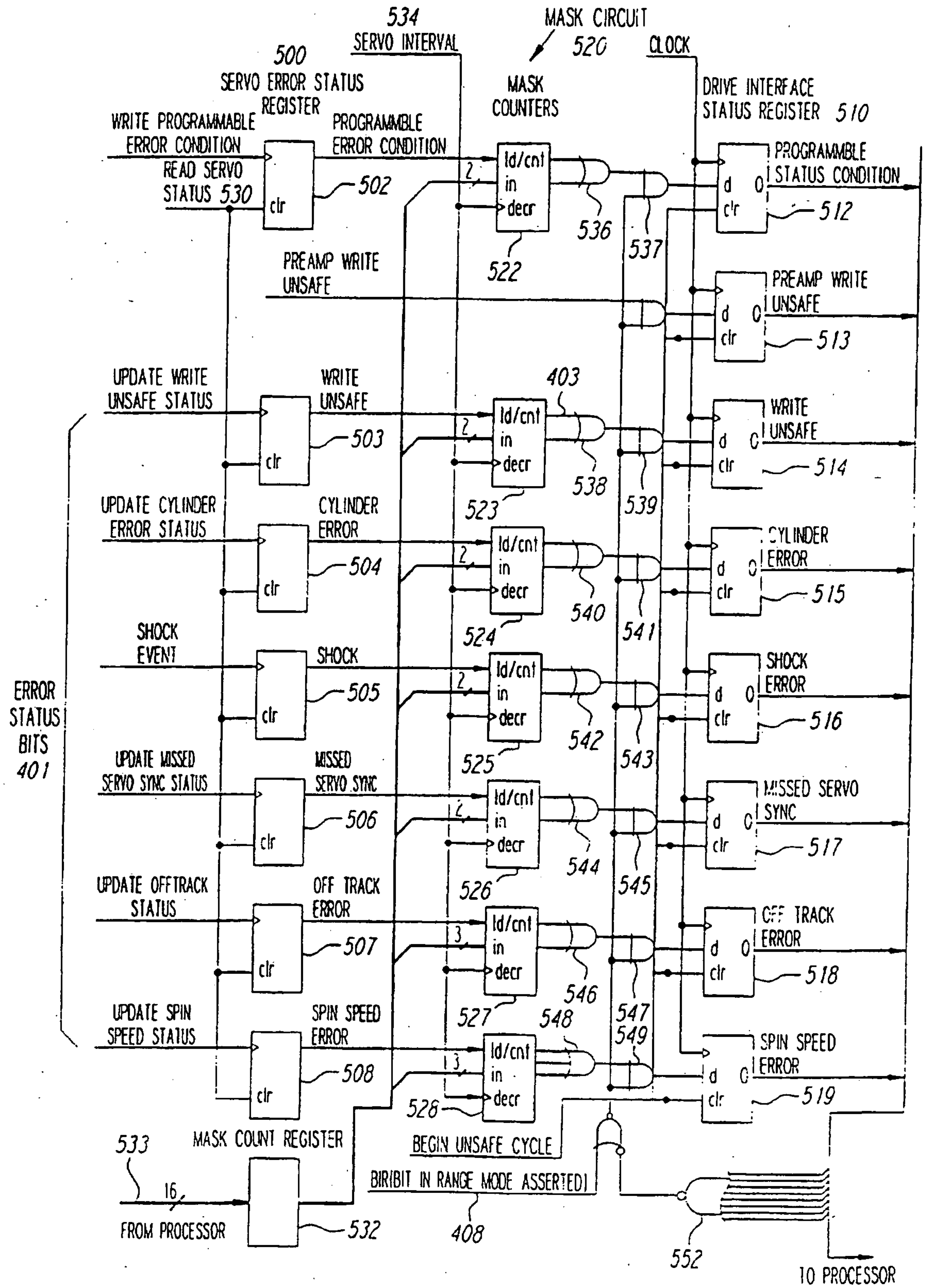

MASK CIRCUIT 402
DRIVE INTERFACE STATUS REGISTER 404
TO MICROPROCESSOR
COUNT VALUES RE: UNMASKED ERROR STATUS BITS 403
406
ERROR STATUS BITS
BIR BIT 408
400 SERVO ERROR STATUS REGISTER
ERROR STATUS BITS 401

FIG. 46



DUAL INTERRUPT STATUS REGISTERS AND MASK HARDWARE

FIG. 47

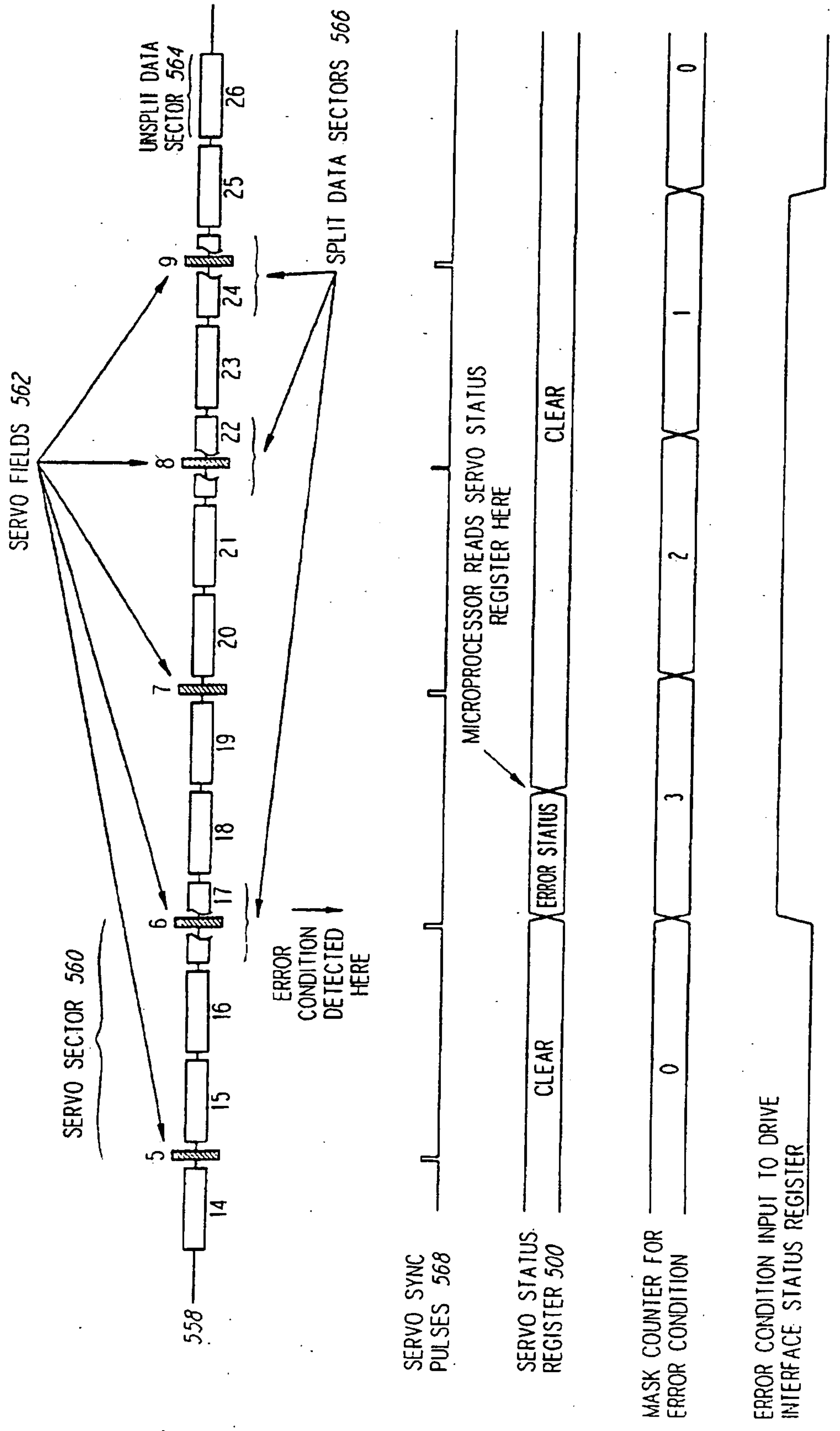

SERVO FIELDS 562
UNSPLIT DATA SECTOR 564
SPLIT DATA SECTORS 566
SERVO SECTOR 560
558
14
5
15
16
6
17
18
19
7
20
21
8
22
23
24
9
25
26
ERROR CONDITION DETECTED HERE
MICROPROCESSOR READS SERVO STATUS REGISTER HERE
SERVO SYNC PULSES 568
SERVO STATUS REGISTER 500
CLEAR
ERROR STATUS
CLEAR
MASK COUNTER FOR ERROR CONDITION
0
3
2
1
0
ERROR CONDITION INPUT TO DRIVE INTERFACE STATUS REGISTER

FIG. 48

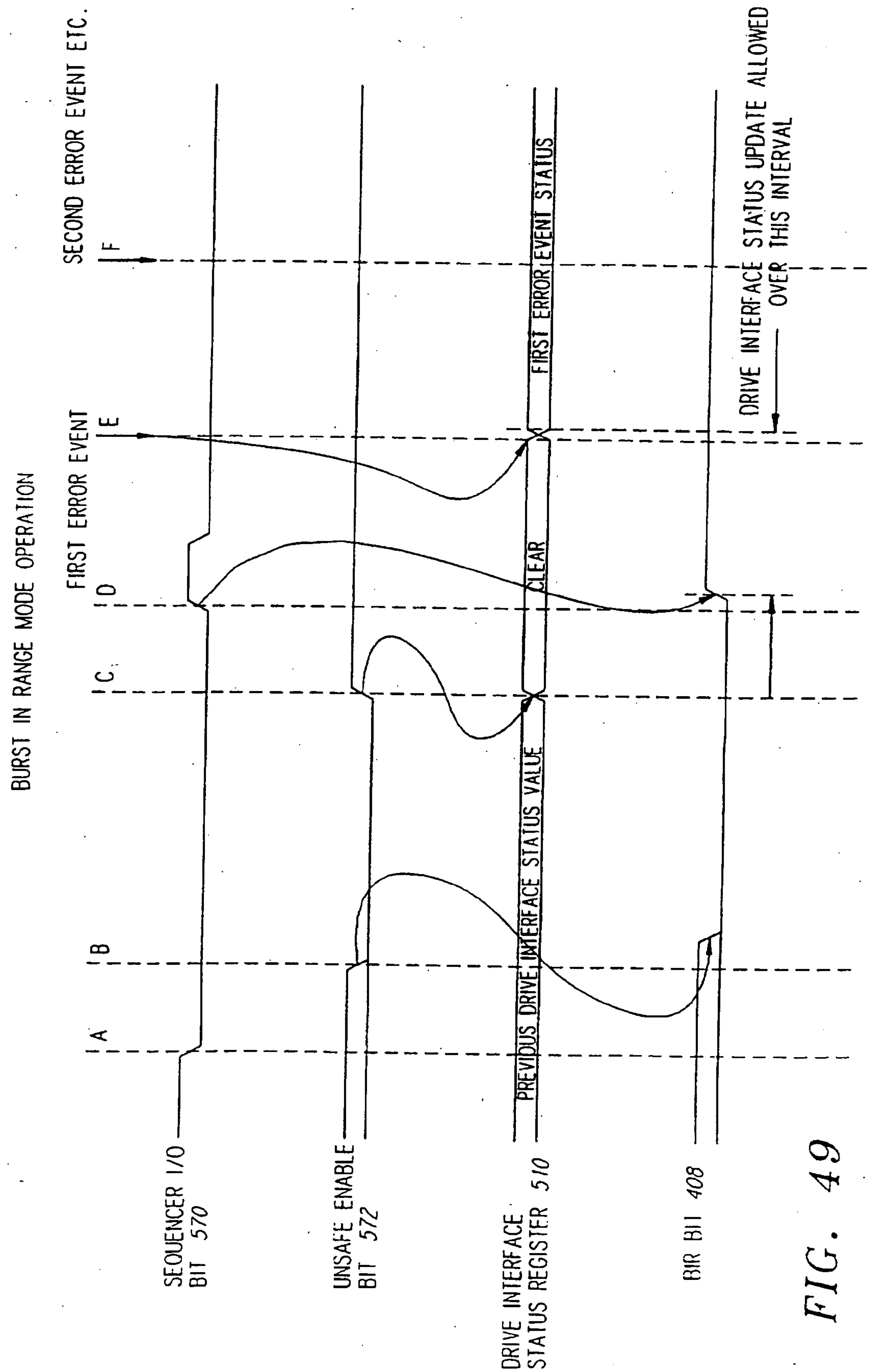

BURST IN RANGE MODE OPERATION
FIRST ERROR EVENT
SECOND ERROR EVENT ETC.
A
B
C
D
E
F
SEQUENCER I/O BIT 570
UNSAFE ENABLE BIT 572
DRIVE INTERFACE STATUS REGISTER 510
BIR BIT 408
PREVIOUS DRIVE INTERFACE STATUS VALUE
CLEAR
FIRST ERROR EVENT STATUS
DRIVE INTERFACE STATUS UPDATE ALLOWED OVER THIS INTERVAL

FIG. 49

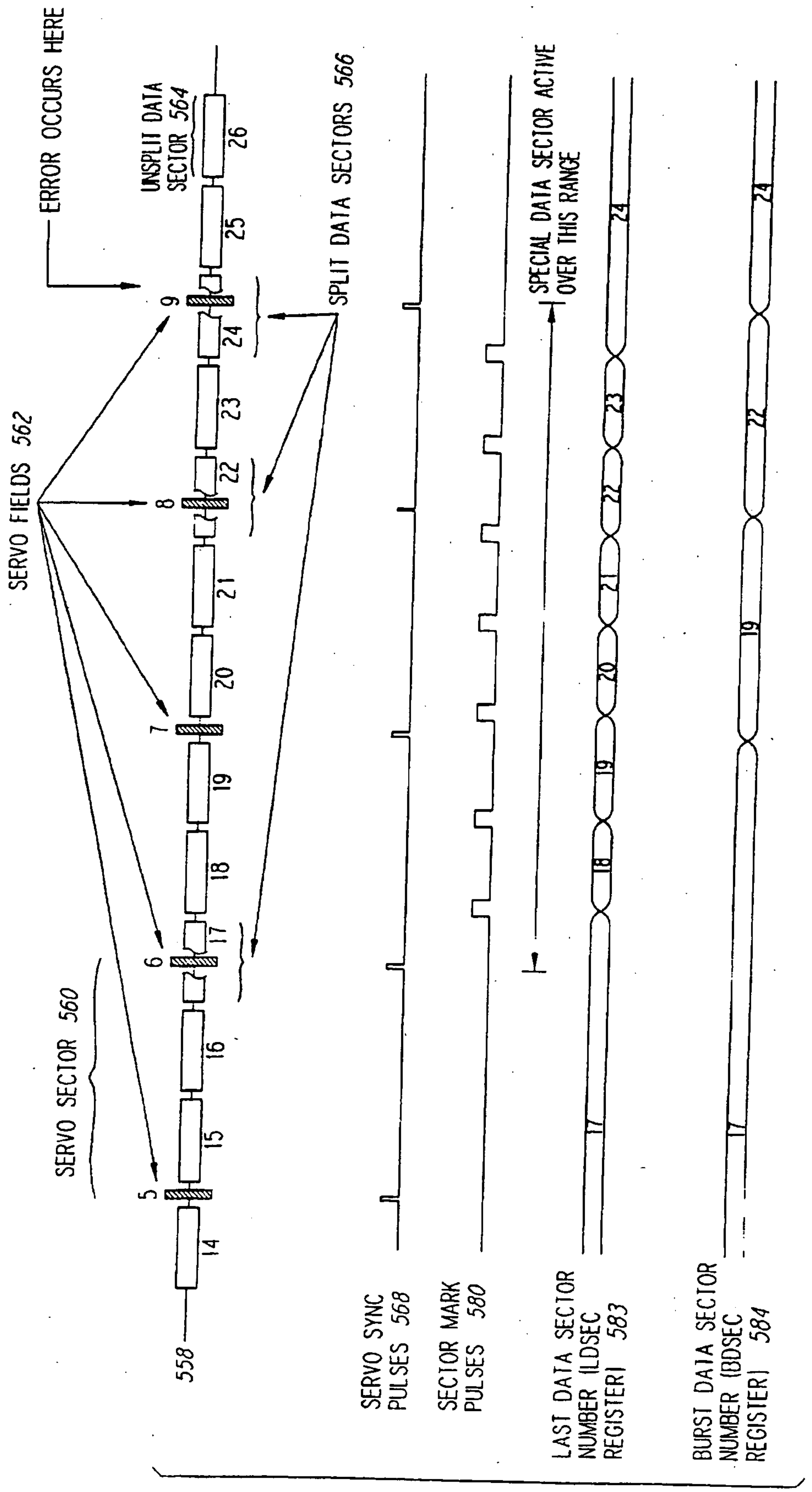

ERROR OCCURS HERE
UNSPLIT DATA SECTOR 564
SPLIT DATA SECTORS 566
SERVO FIELDS 562
SERVO SECTOR 560
SPECIAL DATA SECTOR ACTIVE OVER THIS RANGE
558
SERVO SYNC PULSES 568
SECTOR MARK PULSES 580
LAST DATA SECTOR NUMBER (LDSEC REGISTER) 583
BURST DATA SECTOR NUMBER (BDSEC REGISTER) 584

FIG. 50

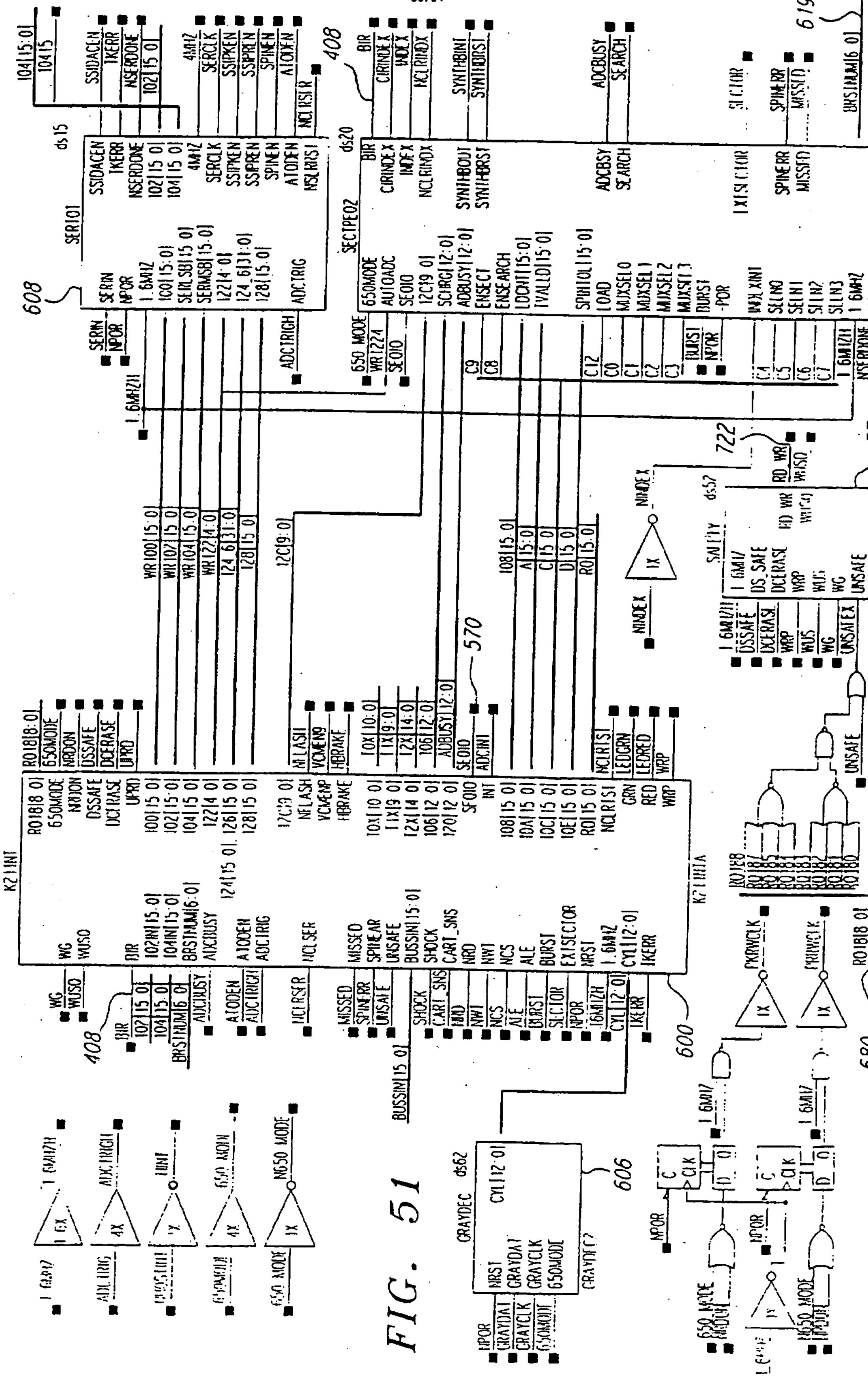


FIG. 51

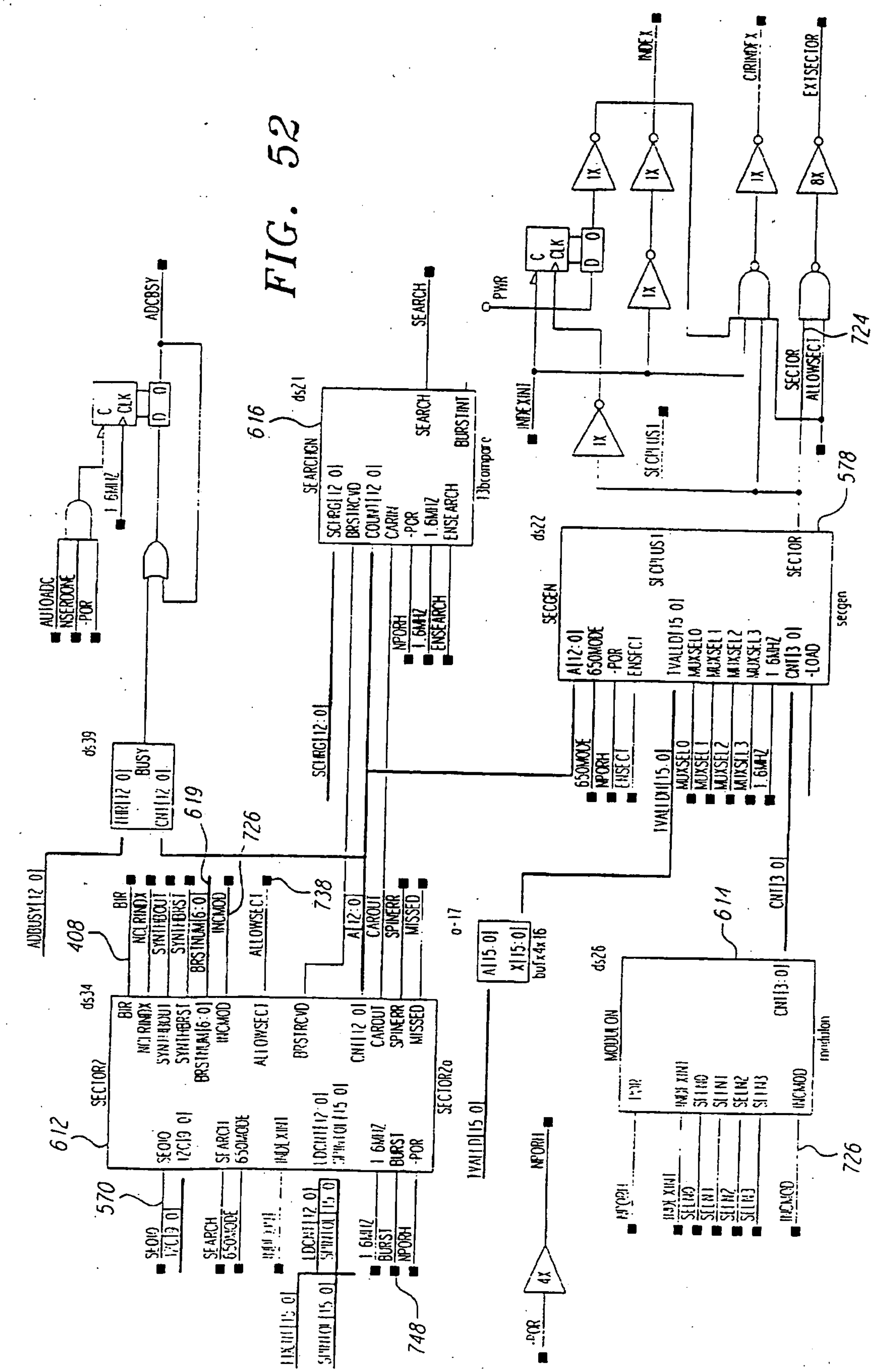

ADCBSY
SEARCH
INDEX
CIRINDEX
EXTSECTOR
PWR
INDEXINT
SECTOR
ALLOWSECT
AUTOADC
NSERDONE
-POR
1.6MHZ
SEARCHGN
13bcompare
SECGEN
sergen
SECTOR2
SECTOR2a
MODULON
modulon
bufx4x16
ADBUSY[12:0]
NPORH
616
408
619
726
738
612
570
748
614
578
724

FIG. 52

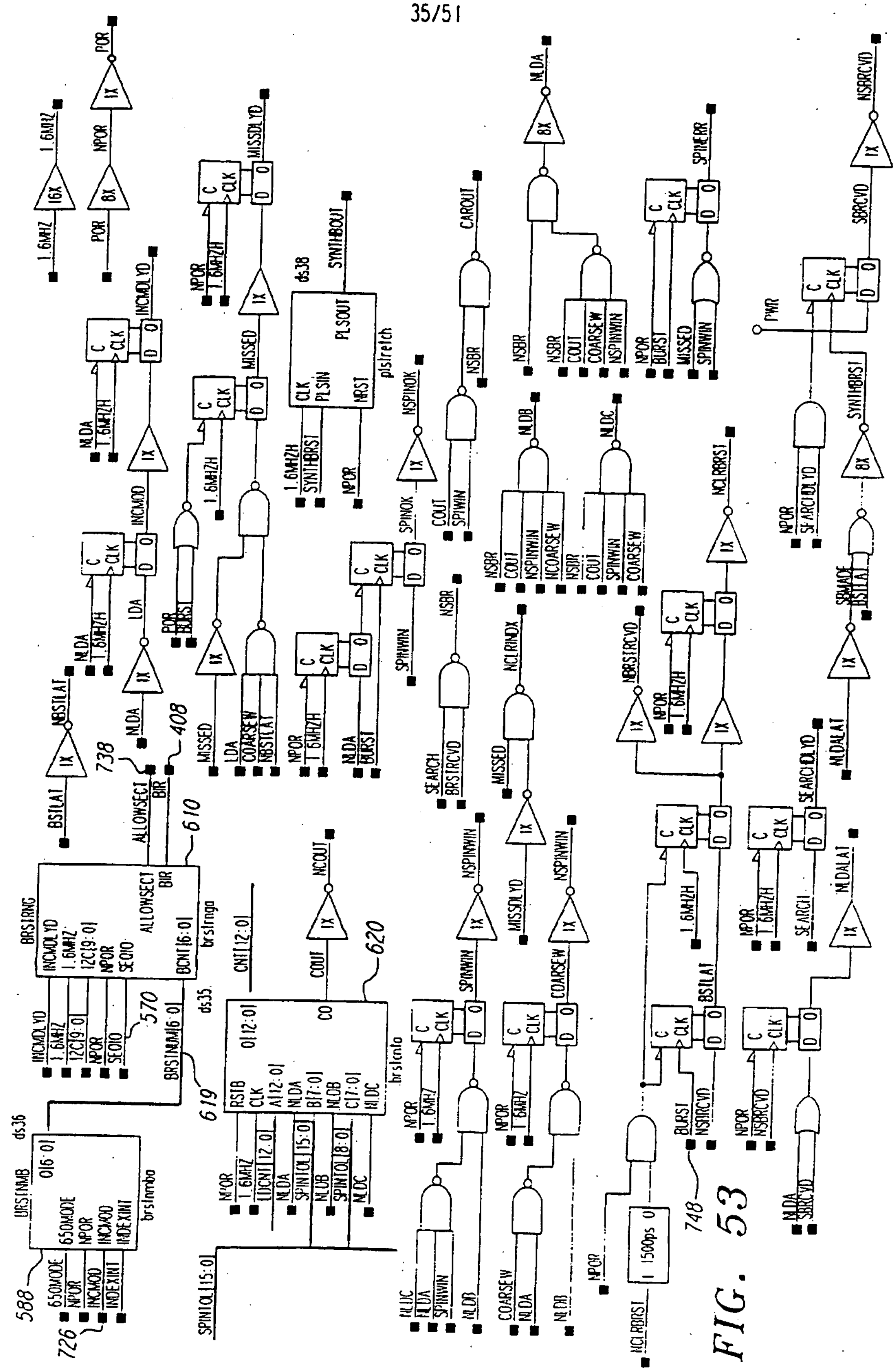


FIG. 53

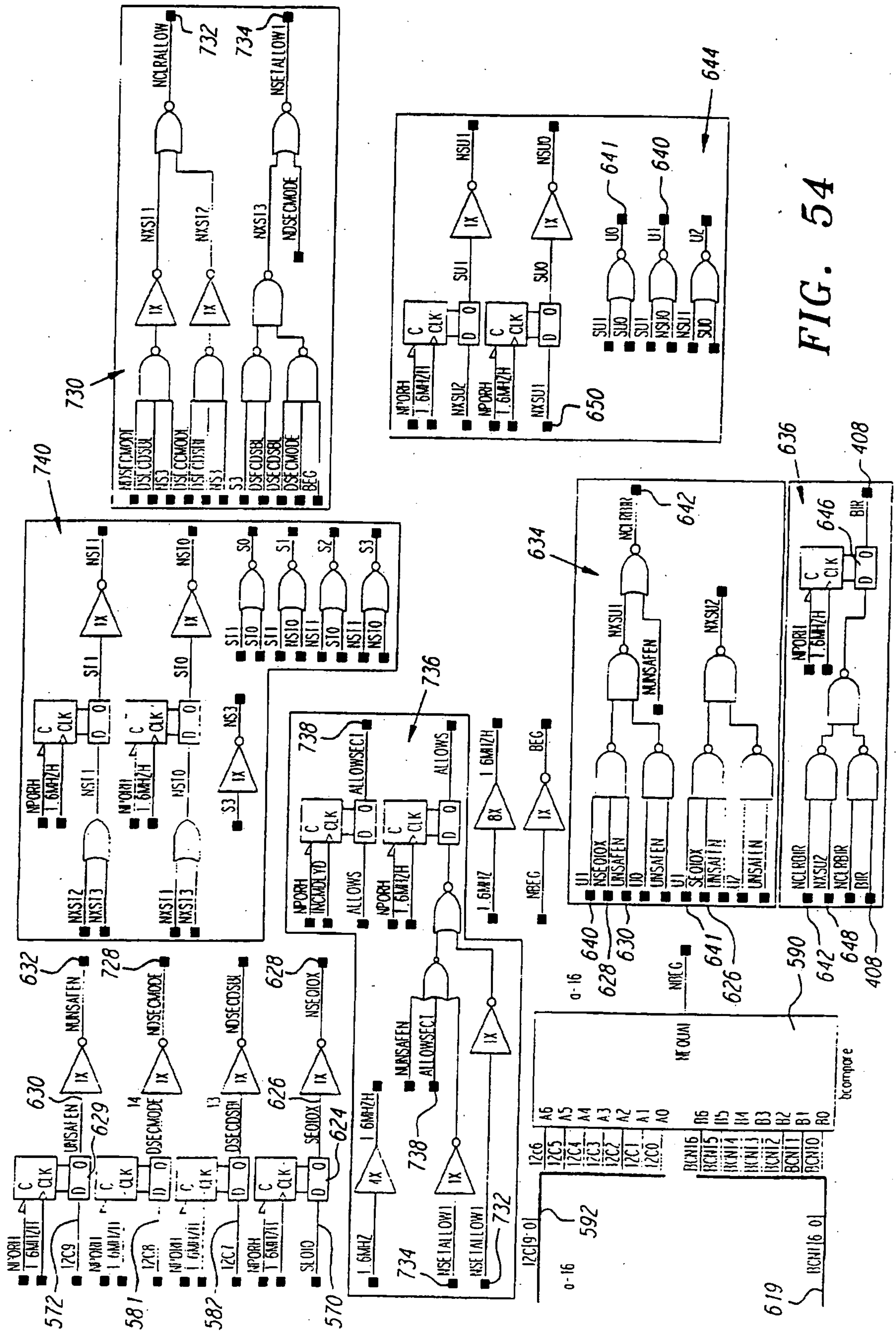

730
740
732
734
NCLRALLOW
NSETALLOW1
NXS11
NXS12
NXS13
NDSECMODE
644
641
640
NSU1
NSU0
SU1
SU0
U0
U1
U2
650
NXSU1
NXSU2
636
408
642
646
BIR
634
NUNSAFEN
736
738
ALLOWSEC1
ALLOWS
1.6MHZH
BEG
NBEG
1.6MHZ
632
728
628
630
629
626
624
NDSECDSBL
NSEQ10X
SEQ10X
572
581
582
570
SLQ10
I2C9
I2C8
I2C7
NPORH
590
bcompare
592
619
I2C[9:0]
BCNT[6:0]
a-16
640
628
630
641
626
642
648
408
NS11
NS10
NS3
S3
S0
S1
S2
ST1
ST0
1X
4X
8X
C
CLK
D
Q

FIG. 54

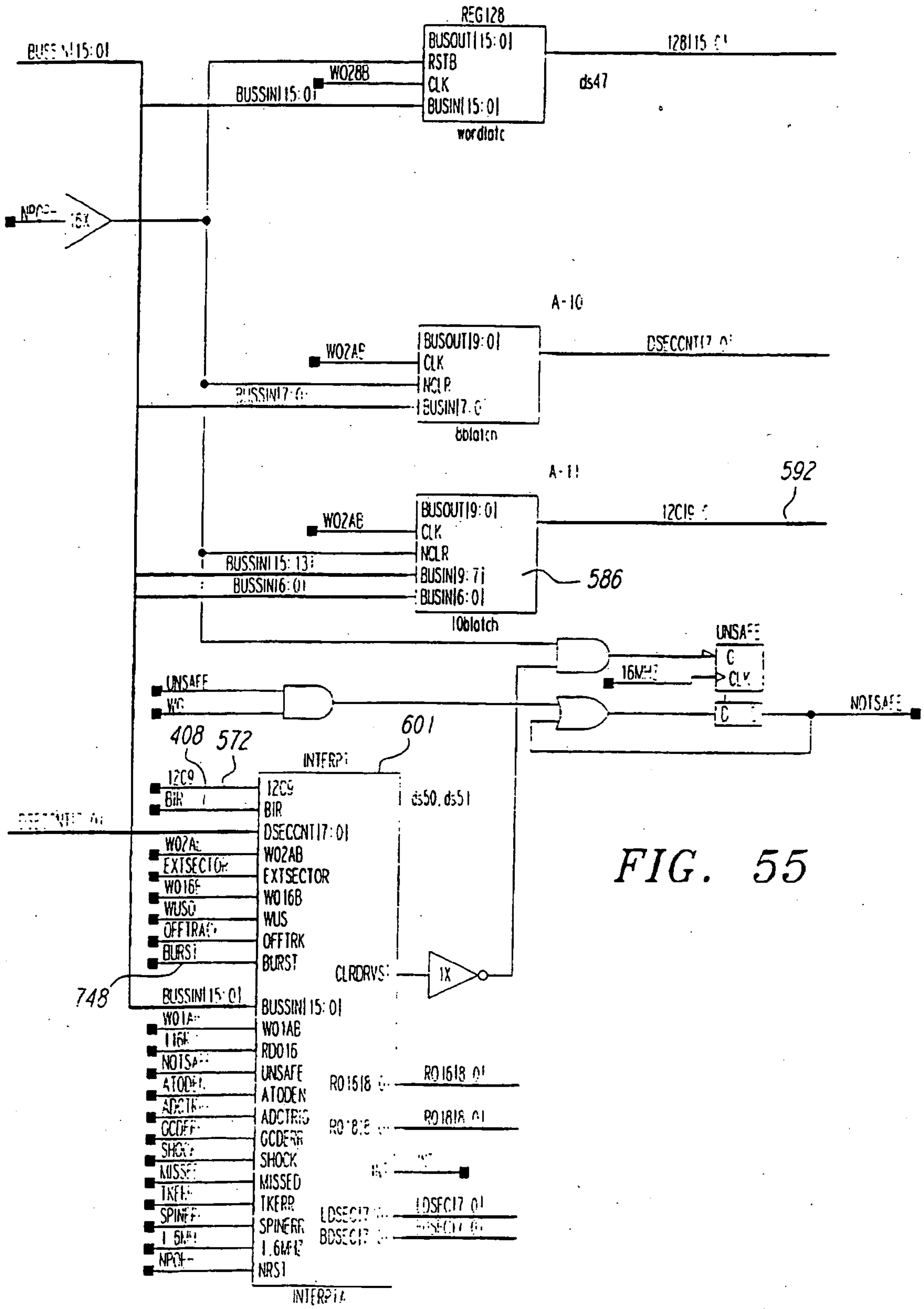

REG128
BUSOUT[15:0]
RSTB
CLK
BUSIN[15:0]
wordlatc
W028B
BUSSIN[15:0]
ds47
16X
A-10
BUSOUT[9:0]
CLK
NCLR
W02AB
8blatch
A-11
592
12C9
586
BUSSIN[15:13]
BUSSIN[6:0]
BUSIN[9:7]
BUSIN[6:0]
10blatch
UNSAFE
16MHZ
CLK
NOTSAFE
601
408
572
INTERP
ds50, ds51
12C9
BIR
DSECCNT[7:0]
W02AB
EXTSECTOR
W016B
WUS
OFFTRK
BURST
CLRDRVS
1X
748
BUSSIN[15:0]
W01AB
RD016
UNSAFE
ATODEN
ADCTRIG
GCDERR
SHOCK
MISSED
TKERR
SPINERR
1.6MHZ
NRST
INTERP1A

FIG. 55

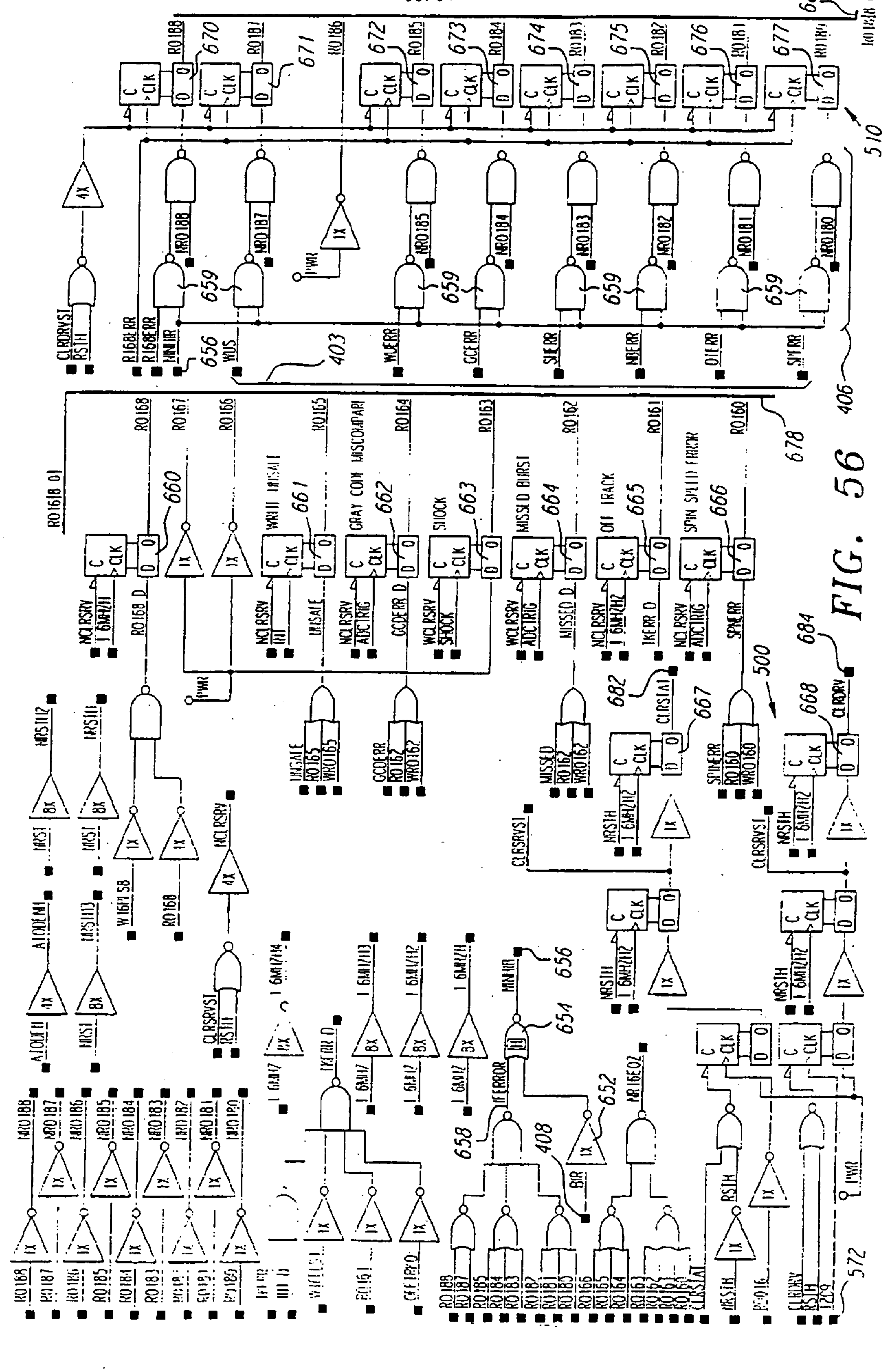


FIG. 56

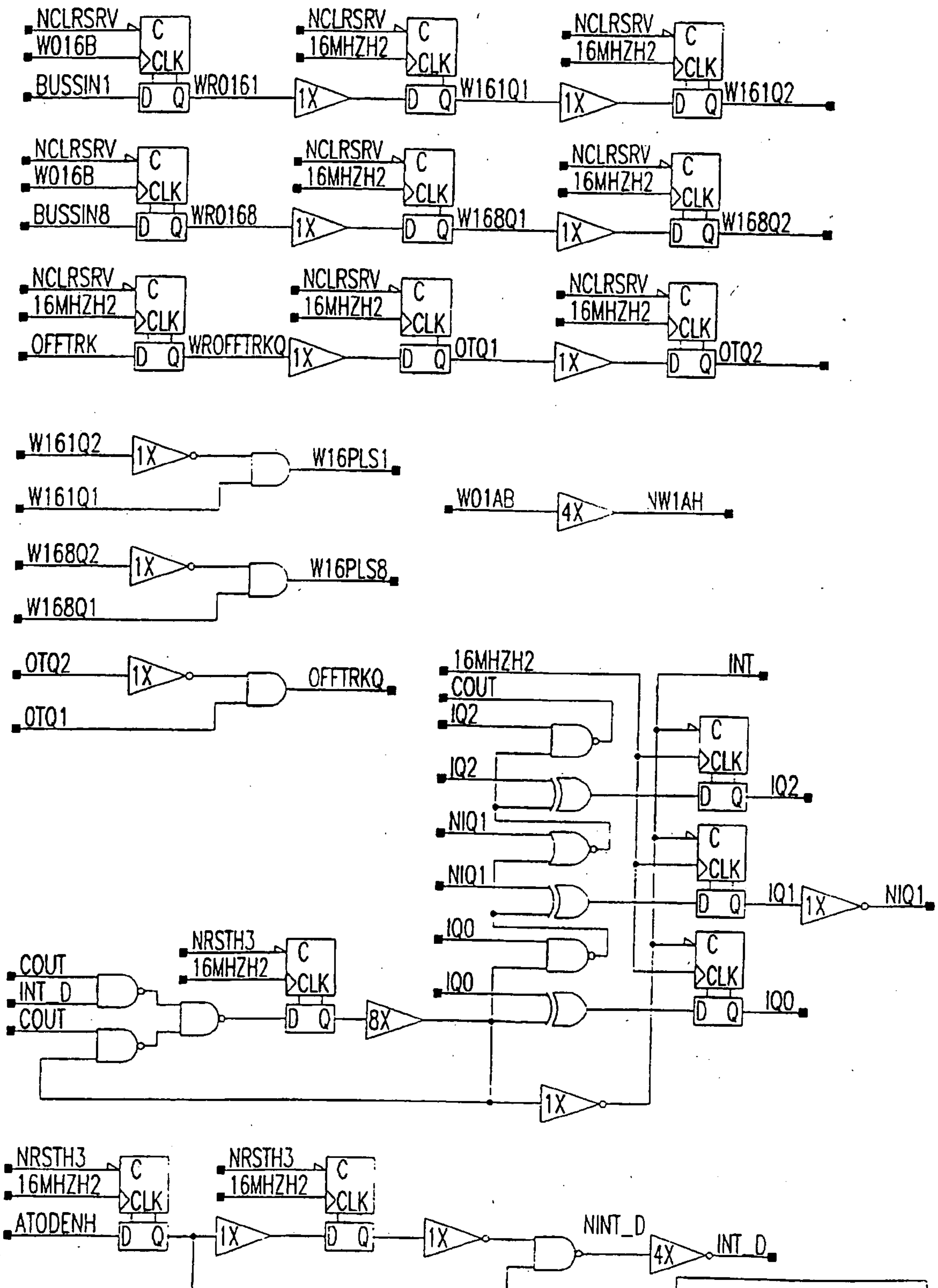


Fig. 57A

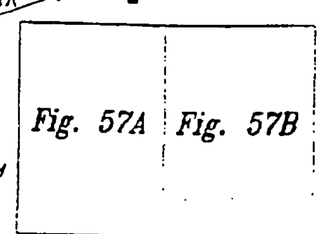


Fig. 57

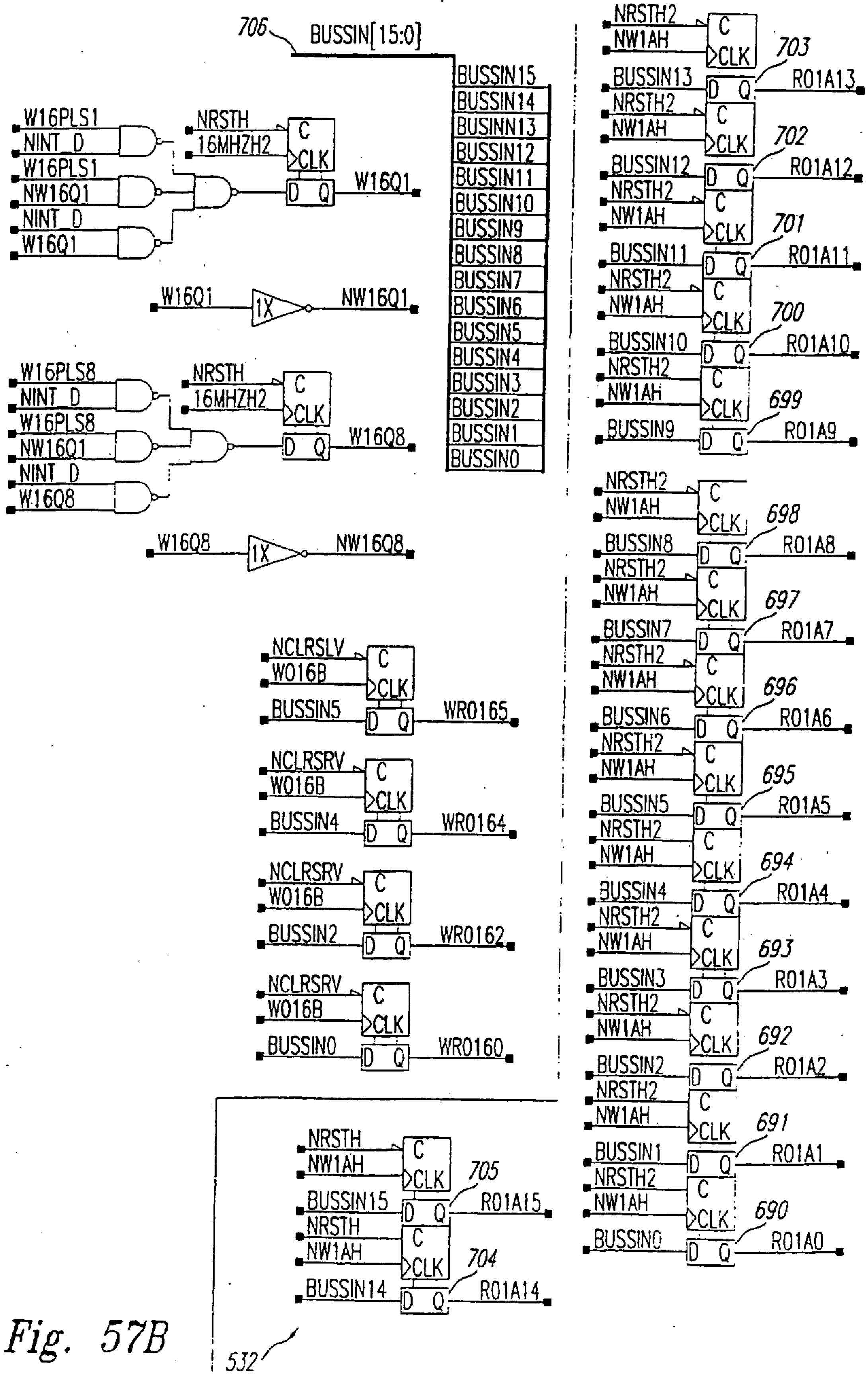

706
BUSSIN[15:0]
BUSSIN15
BUSSIN14
BUSINN13
BUSSIN12
BUSSIN11
BUSSIN10
BUSSIN9
BUSSIN8
BUSSIN7
BUSSIN6
BUSSIN5
BUSSIN4
BUSSIN3
BUSSIN2
BUSSIN1
BUSSIN0
W16PLS1
NINT_D
W16PLS1
NW16Q1
NINT_D
W16Q1
NRSTH
16MHZH2
C
CLK
D Q
W16Q1
W16Q1
1X
NW16Q1
W16PLS8
NINT_D
W16PLS8
NW16Q1
NINT_D
W16Q8
NRSTH
16MHZH2
W16Q8
W16Q8
1X
NW16Q8
NCLRSLV
W016B
BUSSIN5
WR0165
NCLRSRV
W016B
BUSSIN4
WR0164
NCLRSRV
W016B
BUSSIN2
WR0162
NCLRSRV
W016B
BUSSIN0
WR0160
NRSTH
NW1AH
BUSSIN15
705
R01A15
NRSTH
NW1AH
BUSSIN14
704
R01A14
532
NRSTH2
NW1AH
BUSSIN13
703
R01A13
BUSSIN12
702
R01A12
BUSSIN11
701
R01A11
BUSSIN10
700
R01A10
BUSSIN9
699
R01A9
BUSSIN8
698
R01A8
BUSSIN7
697
R01A7
BUSSIN6
696
R01A6
BUSSIN5
695
R01A5
BUSSIN4
694
R01A4
BUSSIN3
693
R01A3
BUSSIN2
692
R01A2
BUSSIN1
691
R01A1
BUSSIN0
690
R01A0

Fig. 57B

FIG. 58A

FIG. 58

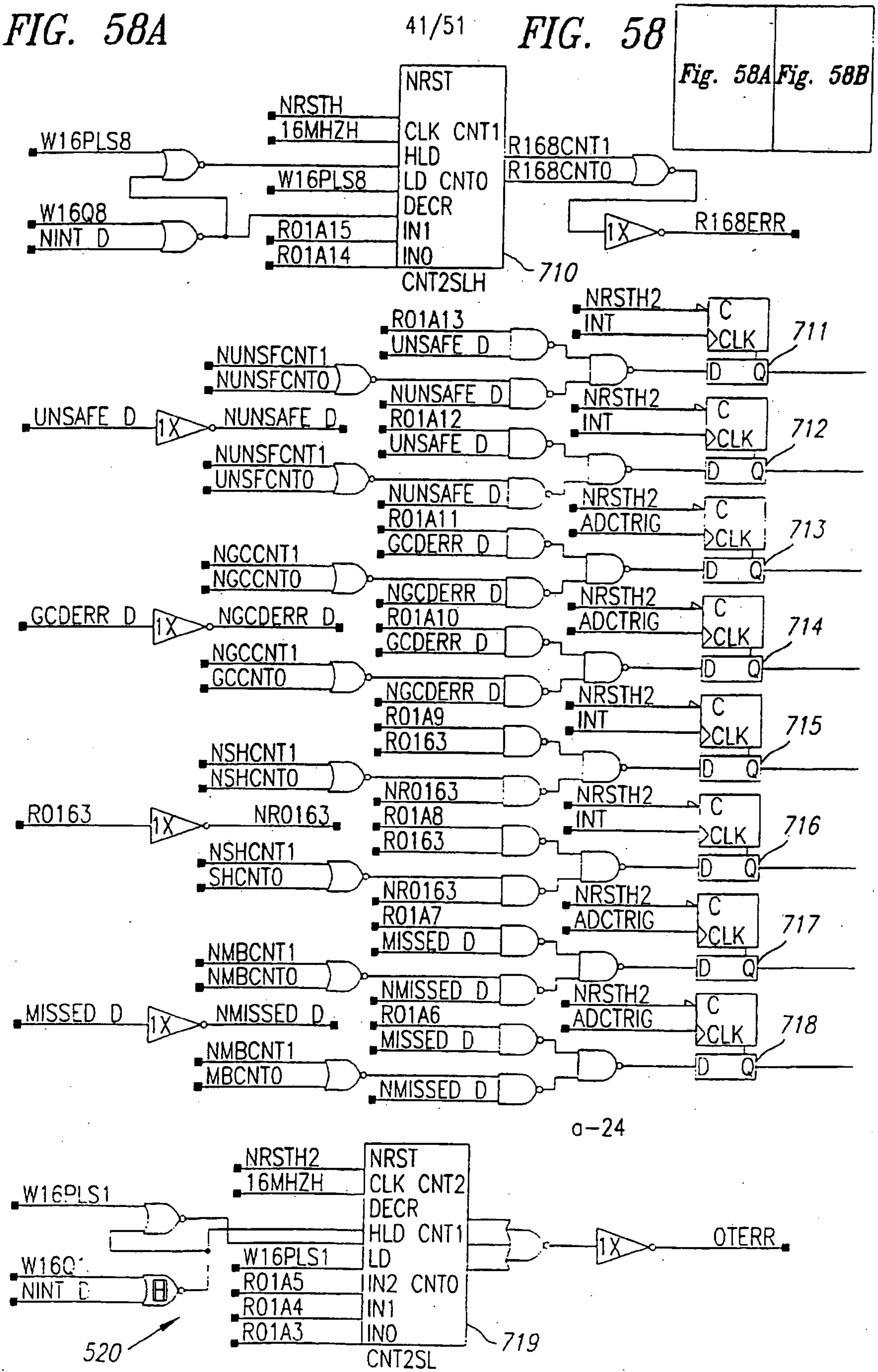


FIG. 58B

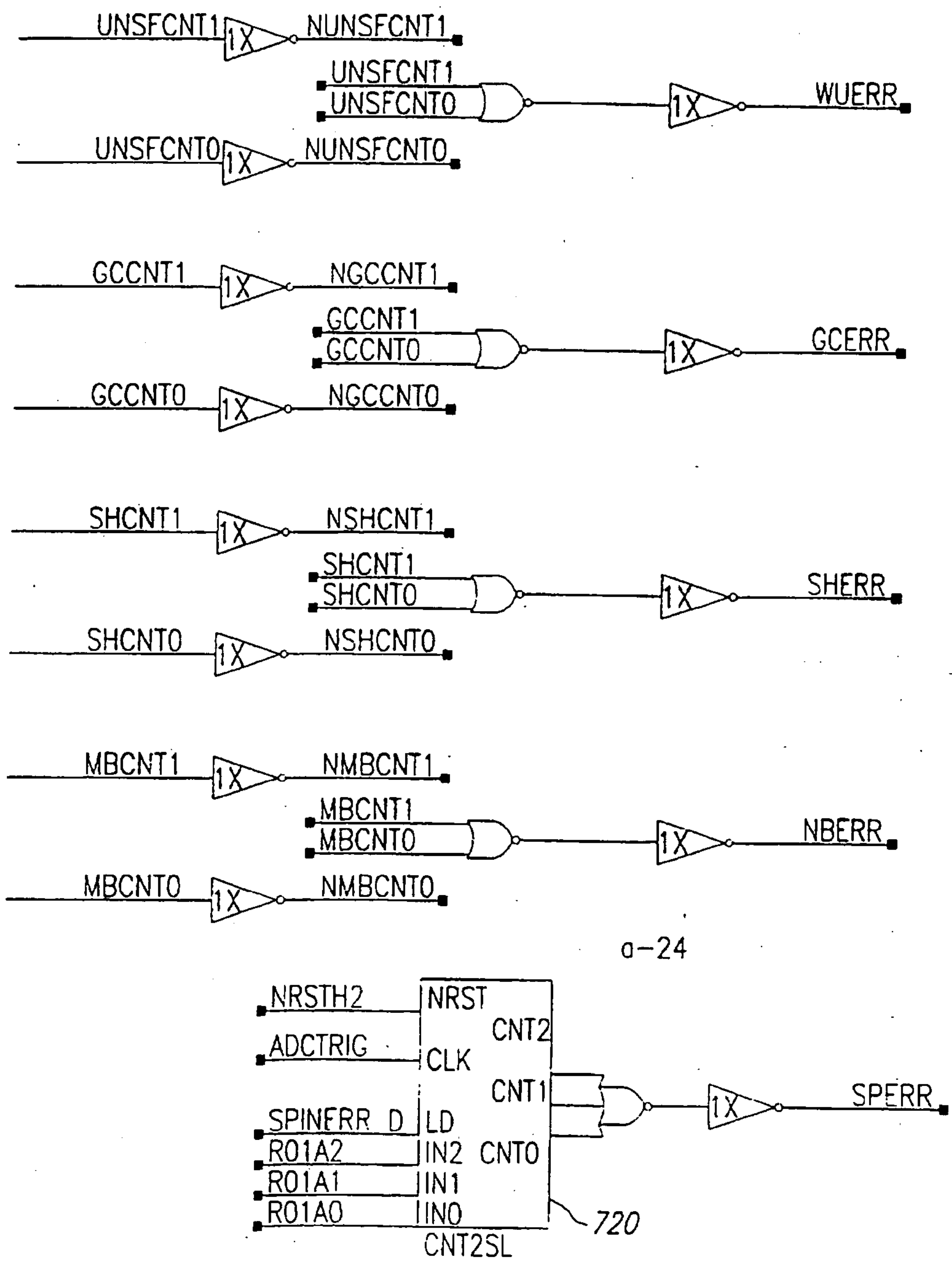

UNSFCNT1
1X
NUNSFCNT1
UNSFCNT1
UNSFCNT0
1X
WUERR
UNSFCNT0
1X
NUNSFCNT0
GCCNT1
1X
NGCCNT1
GCCNT1
GCCNT0
1X
GCERR
GCCNT0
1X
NGCCNT0
SHCNT1
1X
NSHCNT1
SHCNT1
SHCNT0
1X
SHERR
SHCNT0
1X
NSHCNT0
MBCNT1
1X
NMBCNT1
MBCNT1
MBCNT0
1X
NBERR
MBCNT0
1X
NMBCNT0
a-24
NRSTH2
NRST
CNT2
ADCTRIG
CLK
CNT1
SPINERR D
LD
R01A2
IN2
CNT0
R01A1
IN1
R01A0
IN0
CNT2SL
1X
SPERR
720

FIG. 59A

FIG. 59

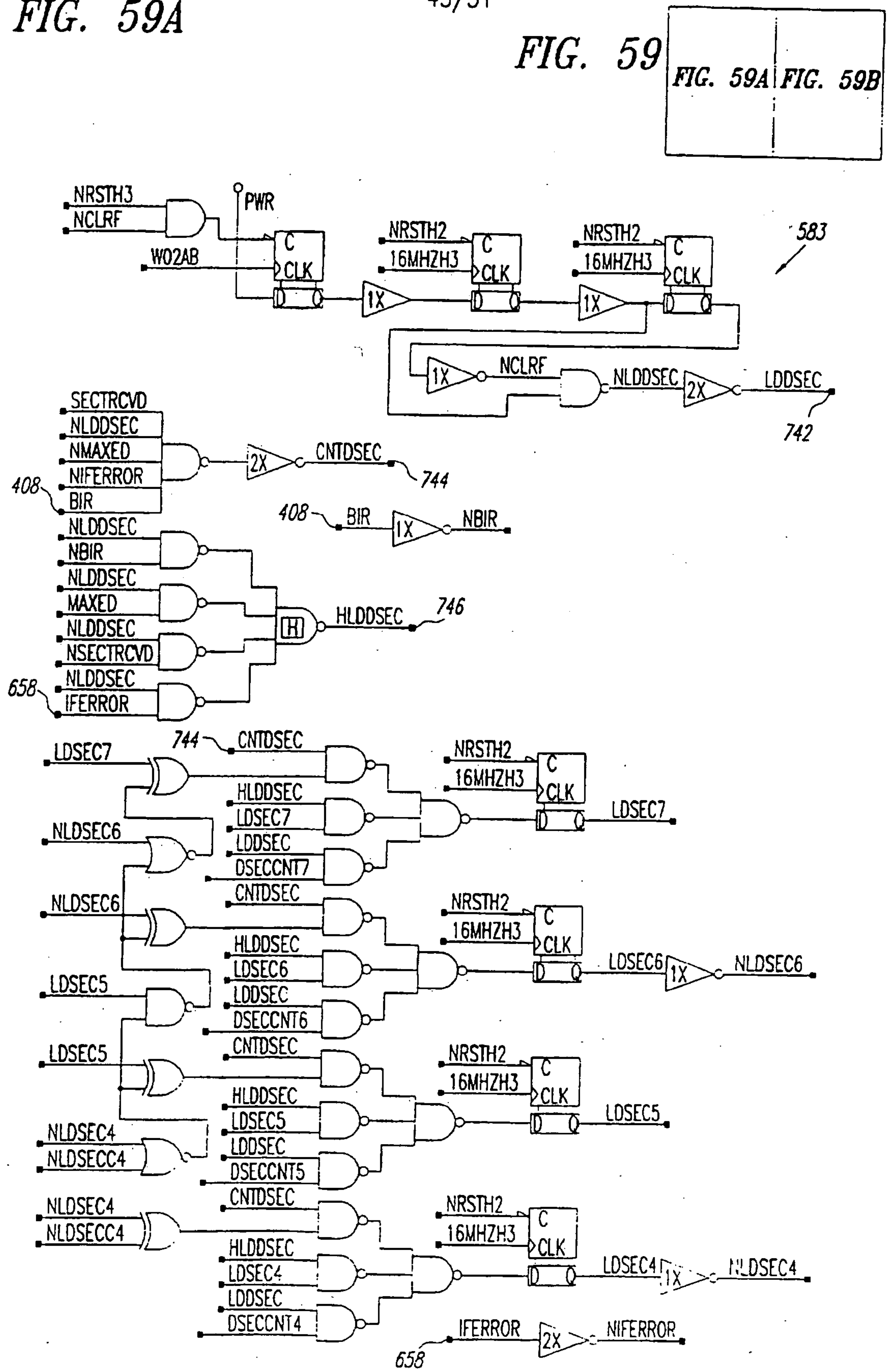
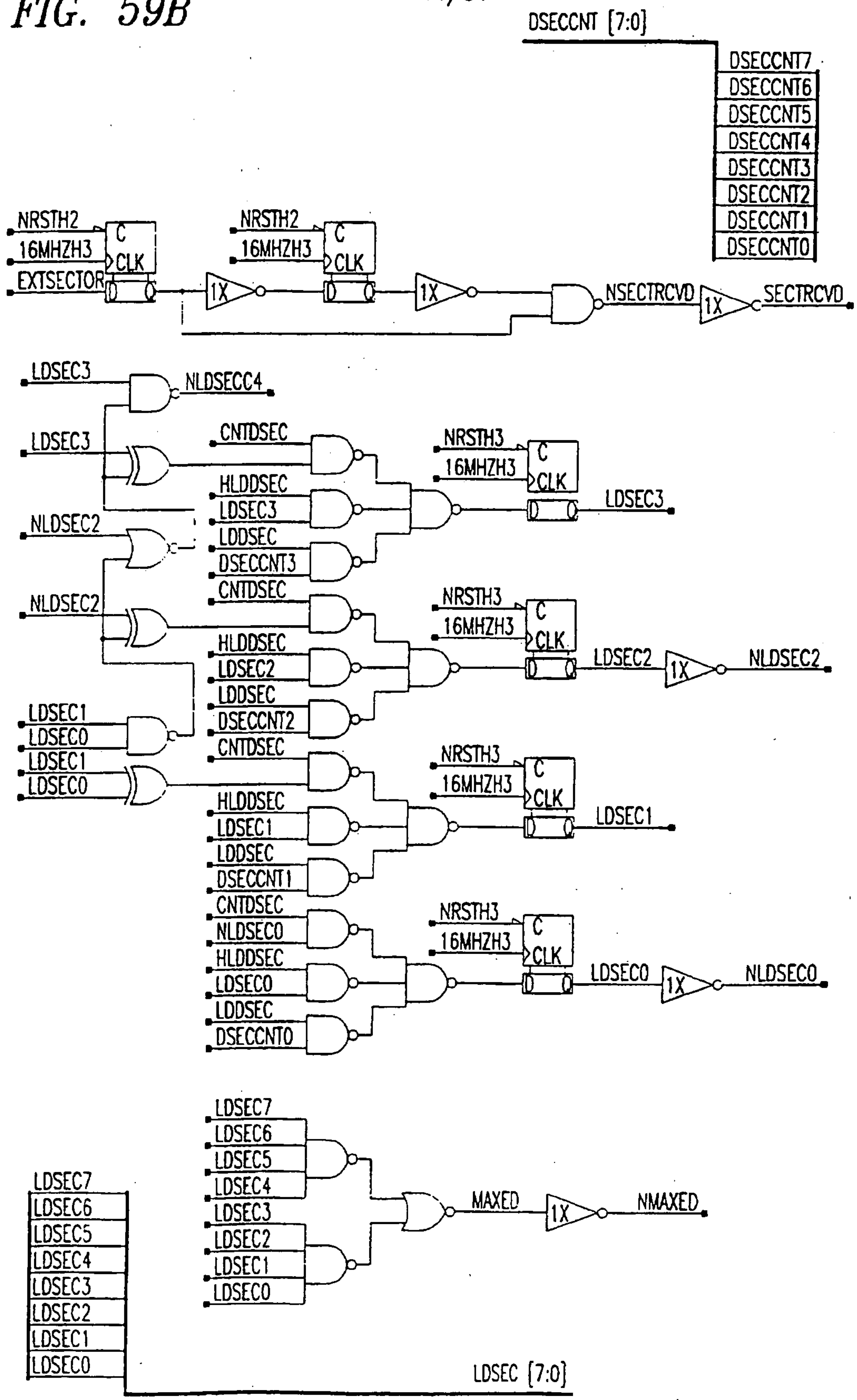


FIG. 59B


DSECCNT [7:0]
DSECCNT7
DSECCNT6
DSECCNT5
DSECCNT4
DSECCNT3
DSECCNT2
DSECCNT1
DSECCNT0
NRSTH2
16MHZH3
EXTSECTOR
C
CLK
D
1X
NSECTRCVD
SECTRCVD
LDSEC3
NLDSECC4
CNTDSEC
HLDDSEC
LDDSEC
NLDSEC2
NRSTH3
LDSEC2
LDSEC1
LDSEC0
NLDSEC0
LDSEC7
LDSEC6
LDSEC5
LDSEC4
MAXED
NMAXED
LDSEC [7:0]

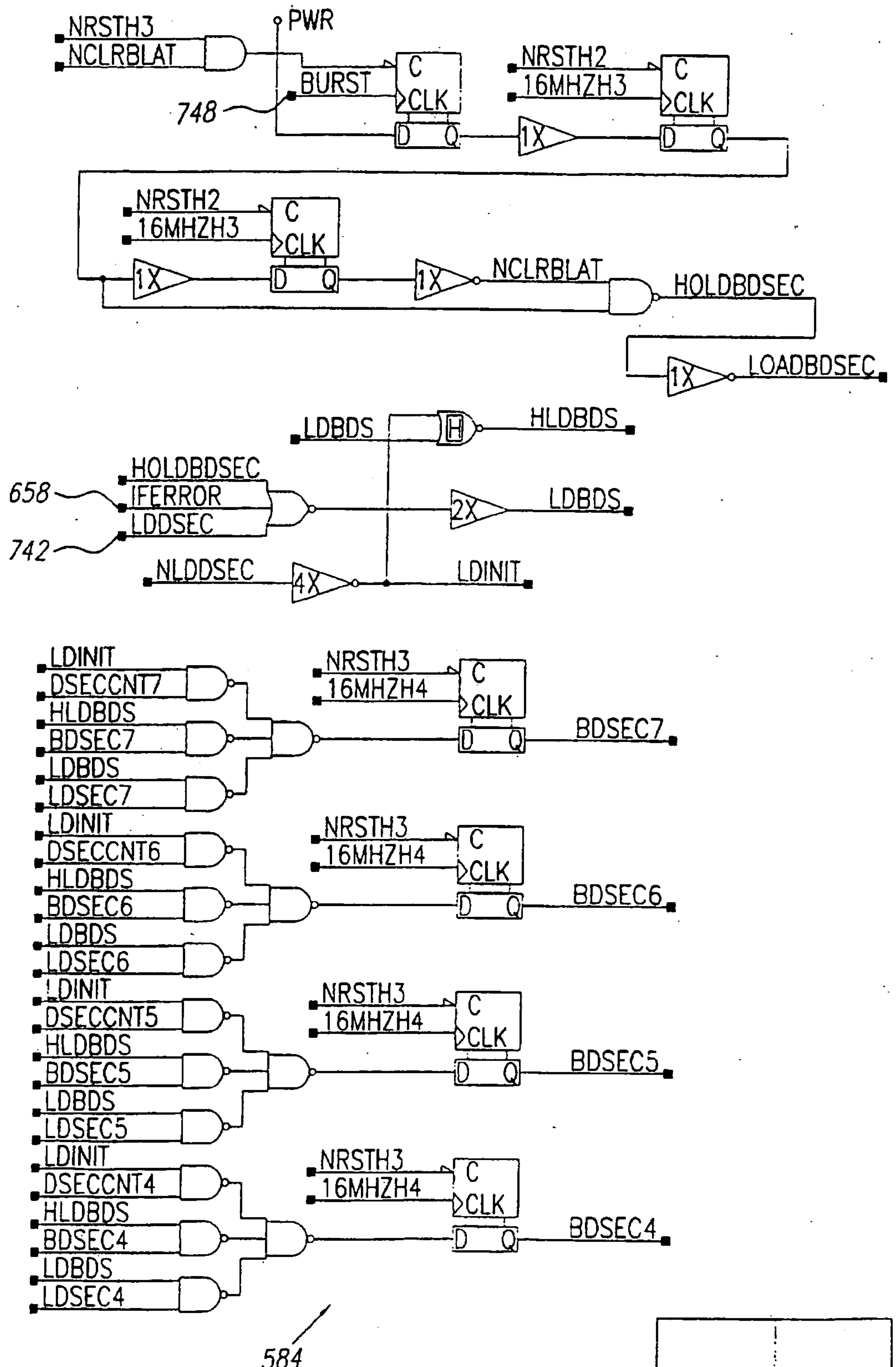


FIG. 60A

FIG. 60

FIG. 60A	FIG. 60B

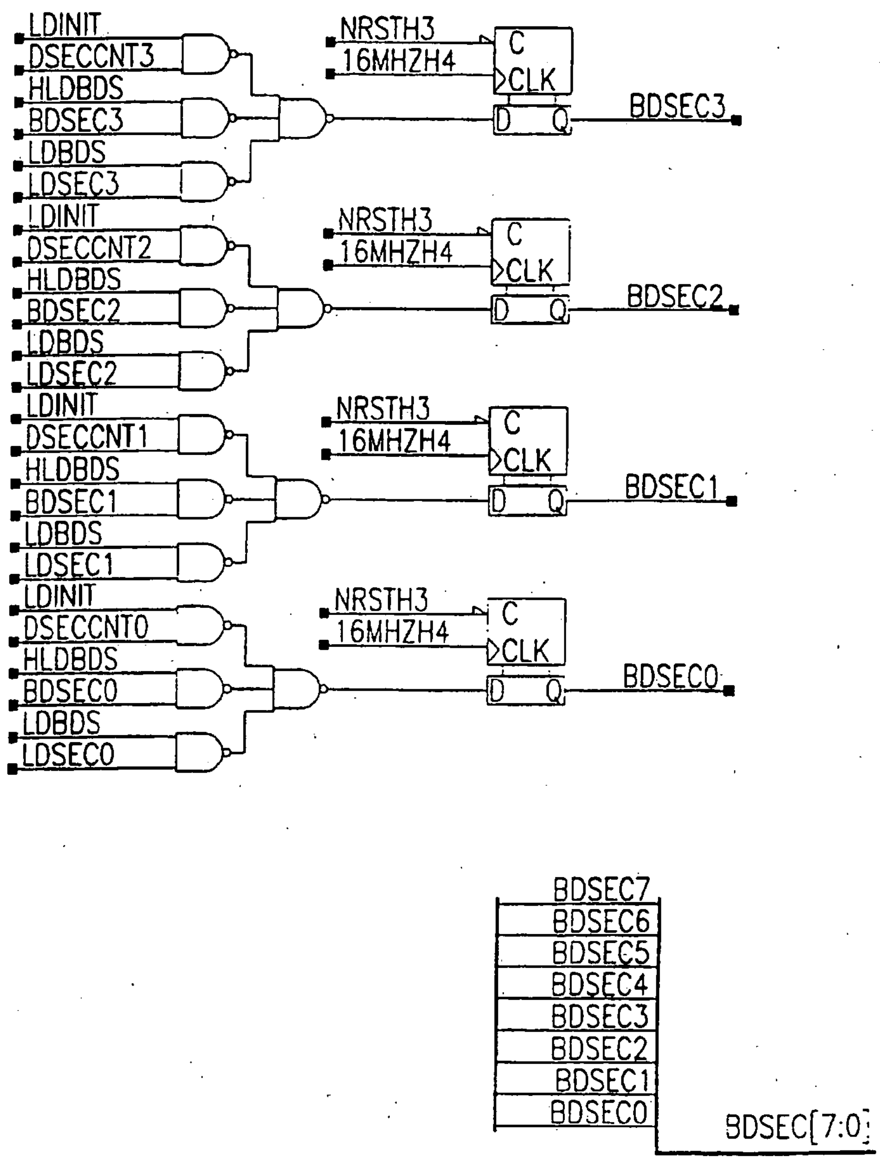

LDINIT
DSECCNT3
HLDBDS
BDSEC3
LDBDS
LDSEC3
NRSTH3
16MHZH4
C
CLK
D
Q
BDSEC3
LDINIT
DSECCNT2
HLDBDS
BDSEC2
LDBDS
LDSEC2
NRSTH3
16MHZH4
BDSEC2
LDINIT
DSECCNT1
HLDBDS
BDSEC1
LDBDS
LDSEC1
NRSTH3
16MHZH4
BDSEC1
LDINIT
DSECCNT0
HLDBDS
BDSEC0
LDBDS
LDSEC0
NRSTH3
16MHZH4
BDSEC0
BDSEC7
BDSEC6
BDSEC5
BDSEC4
BDSEC3
BDSEC2
BDSEC1
BDSEC0
BDSEC[7:0]

FIG. 60B

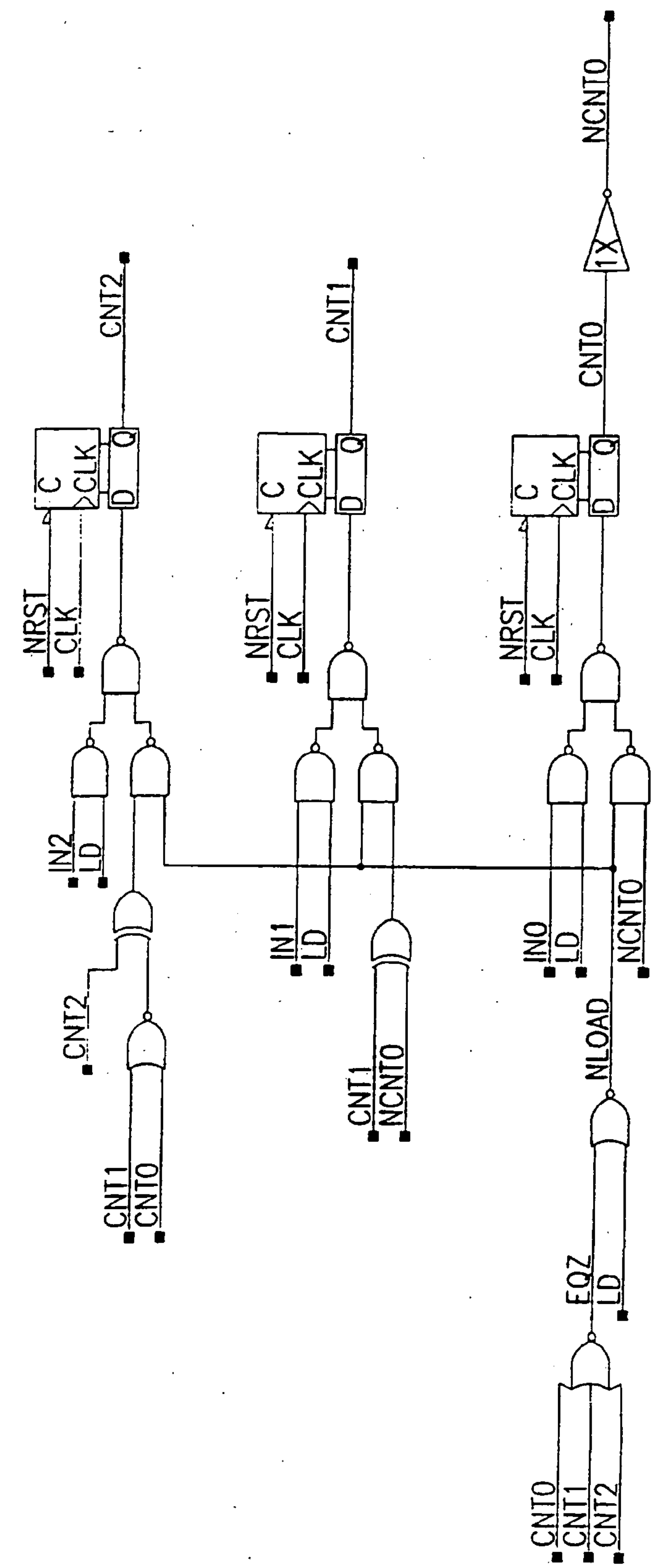

NCNT0
1X
CNT2
CNT1
CNT0
C
CLK
D
Q
NRST
CLK
IN2
LD
CNT2
CNT1
CNT0
IN1
LD
CNT1
NCNT0
IN0
LD
NCNT0
NLOAD
EQZ
LD
CNT0
CNT1
CNT2

FIG. 61

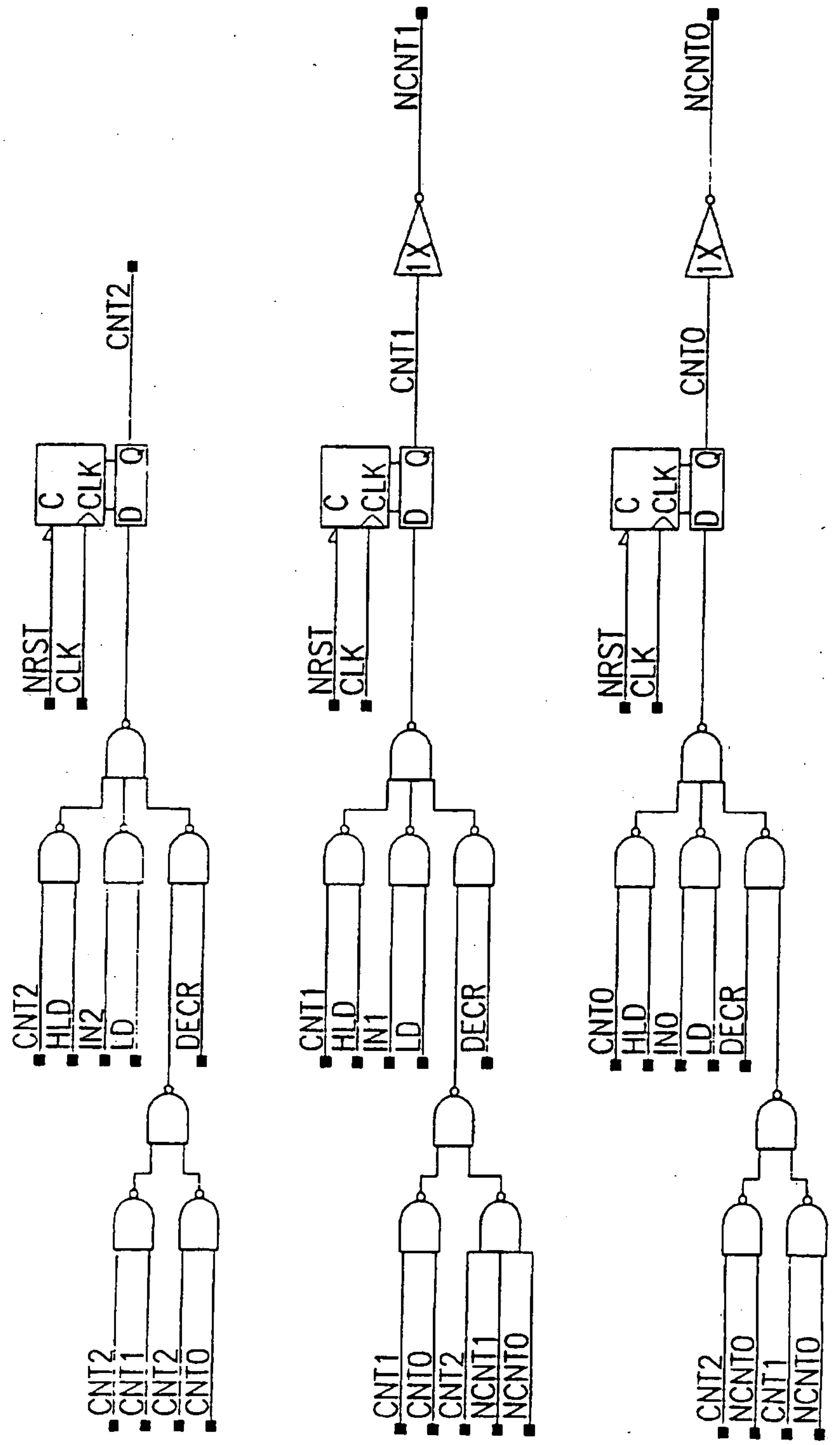

CNT2
NCNT1
NCNT0
1X
1X
CNT1
CNT0
C
CLK
D
Q
C
CLK
D
Q
C
CLK
D
Q
NRST
CLK
NRST
CLK
NRST
CLK
CNT2
HLD
IN2
LD
DECR
CNT1
HLD
IN1
LD
DECR
CNT0
HLD
IN0
LD
DECR
CNT2
CNT1
CNT2
CNT0
CNT1
CNT0
CNT2
NCNT1
NCNT0
CNT2
NCNT0
CNT1
NCNT0

FIG. 62

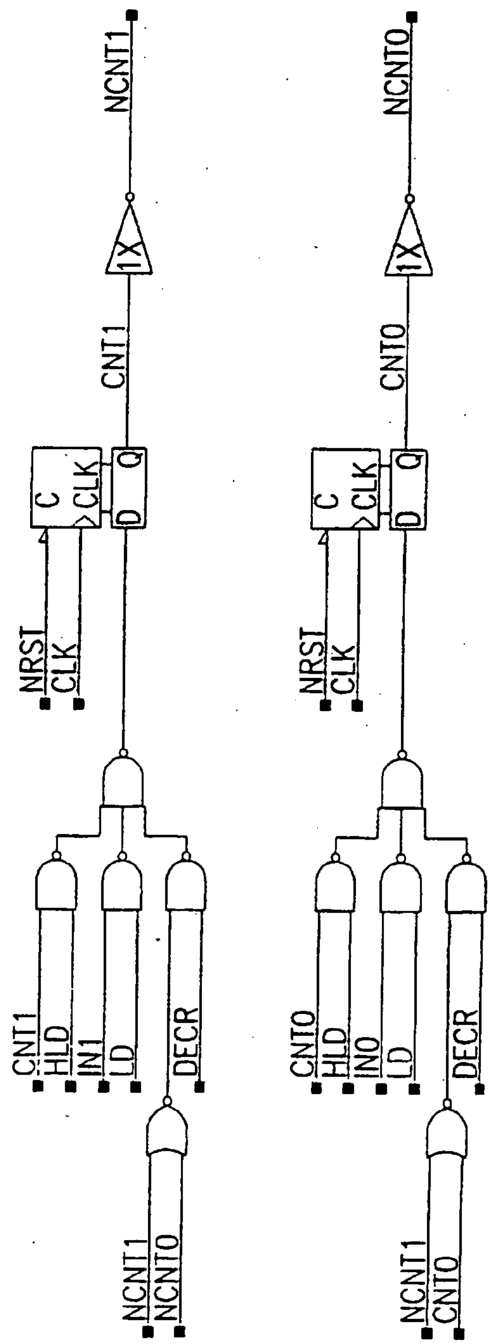

NCNT1
NCNT0
1X
1X
CNT1
CNT0
C
CLK
D
Q
C
CLK
D
Q
NRST
CLK
NRST
CLK
CNT1
HLD
IN1
LD
DECR
CNT0
HLD
IN0
LD
DECR
NCNT1
NCNT0
NCNT1
CNT0

FIG. 63

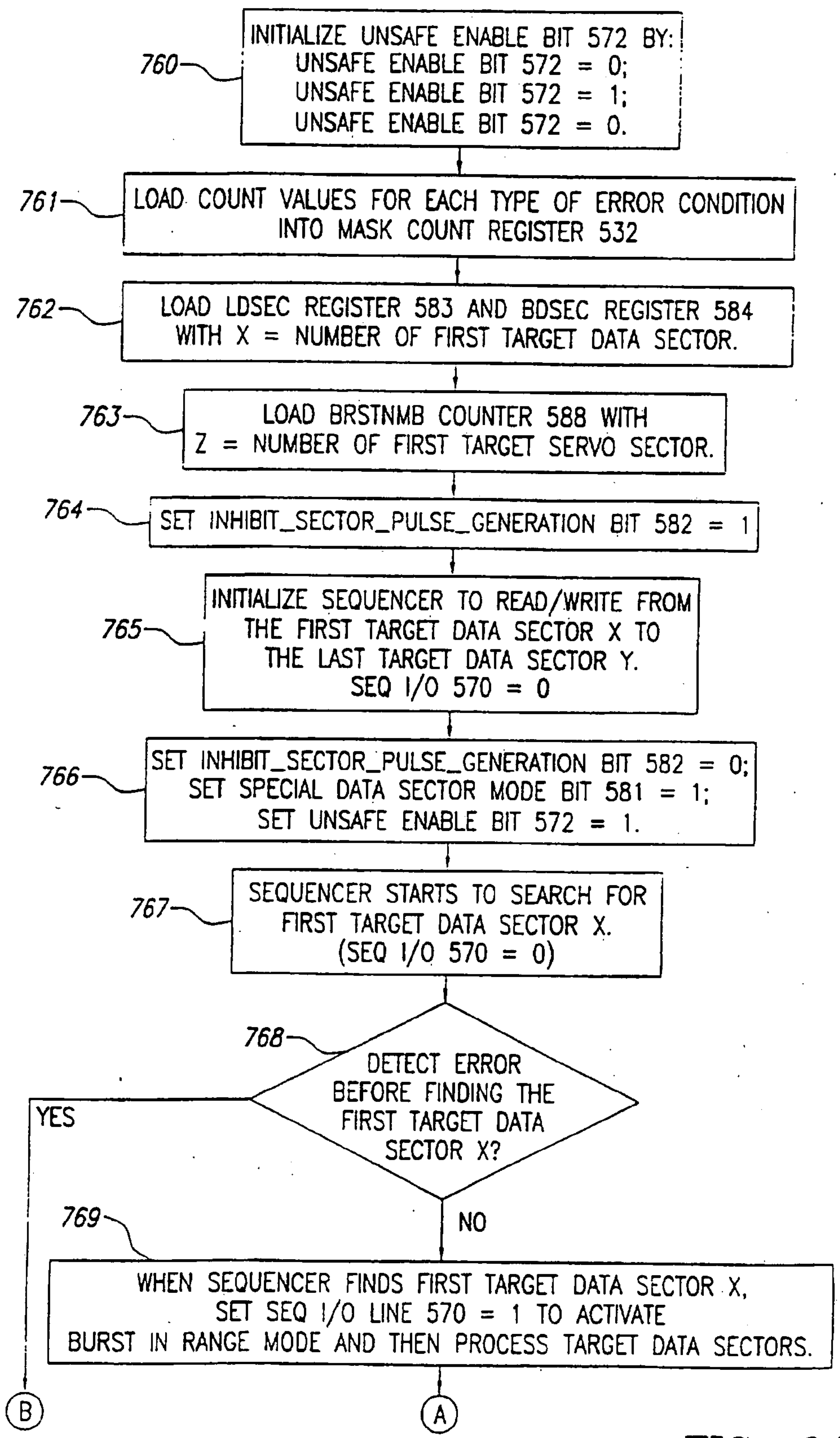

760
INITIALIZE UNSAFE ENABLE BIT 572 BY:
UNSAFE ENABLE BIT 572 = 0;
UNSAFE ENABLE BIT 572 = 1;
UNSAFE ENABLE BIT 572 = 0.
761
LOAD COUNT VALUES FOR EACH TYPE OF ERROR CONDITION INTO MASK COUNT REGISTER 532
762
LOAD LDSEC REGISTER 583 AND BDSEC REGISTER 584 WITH X = NUMBER OF FIRST TARGET DATA SECTOR.
763
LOAD BRSTNMB COUNTER 588 WITH Z = NUMBER OF FIRST TARGET SERVO SECTOR.
764
SET INHIBIT_SECTOR_PULSE_GENERATION BIT 582 = 1
765
INITIALIZE SEQUENCER TO READ/WRITE FROM THE FIRST TARGET DATA SECTOR X TO THE LAST TARGET DATA SECTOR Y. SEQ I/O 570 = 0
766
SET INHIBIT_SECTOR_PULSE_GENERATION BIT 582 = 0; SET SPECIAL DATA SECTOR MODE BIT 581 = 1; SET UNSAFE ENABLE BIT 572 = 1.
767
SEQUENCER STARTS TO SEARCH FOR FIRST TARGET DATA SECTOR X. (SEQ I/O 570 = 0)
768
DETECT ERROR BEFORE FINDING THE FIRST TARGET DATA SECTOR X?
YES
NO
769
WHEN SEQUENCER FINDS FIRST TARGET DATA SECTOR X, SET SEQ I/O LINE 570 = 1 TO ACTIVATE BURST IN RANGE MODE AND THEN PROCESS TARGET DATA SECTORS.
B
A

FIG. 64A

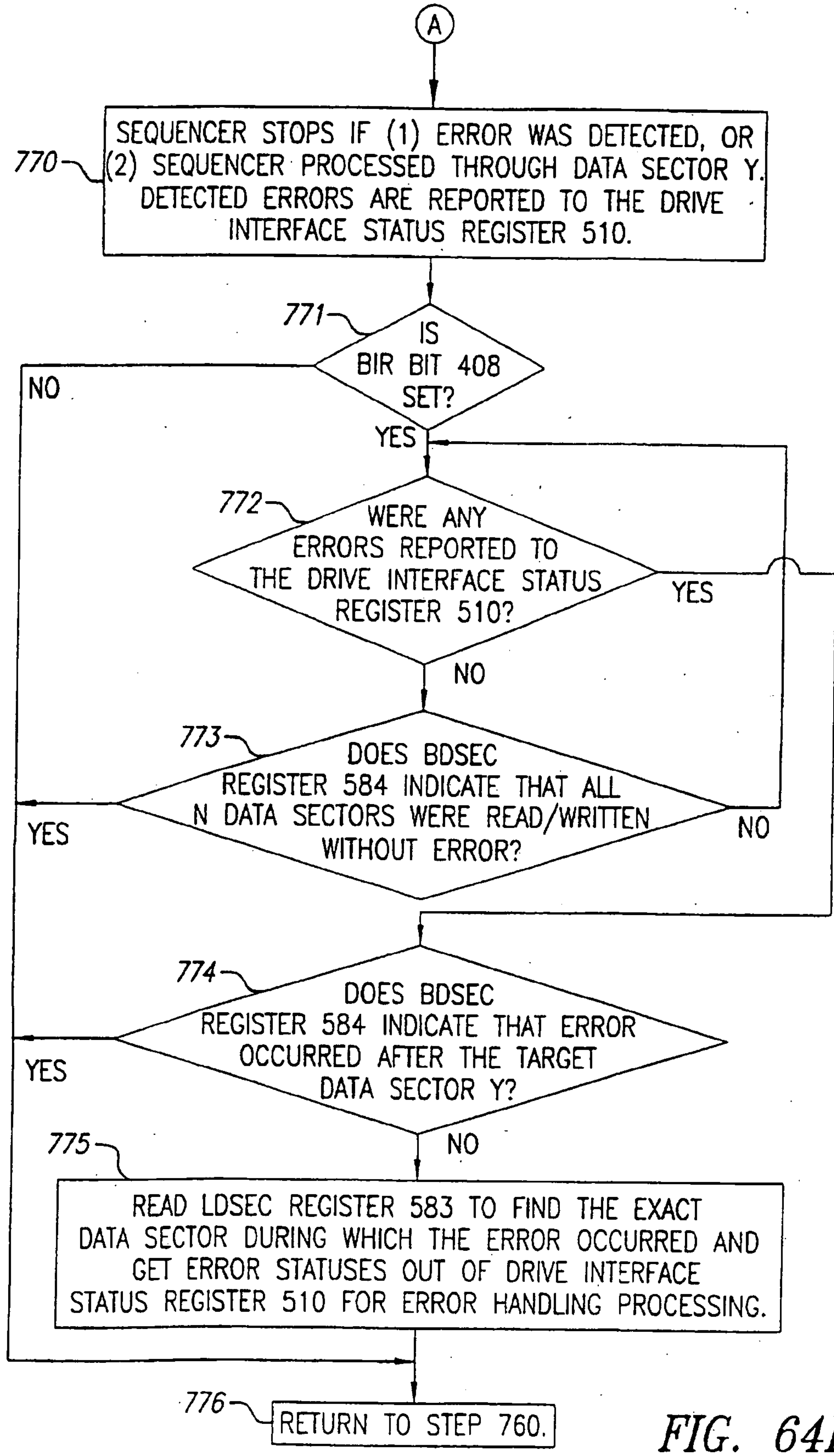

A
770
SEQUENCER STOPS IF (1) ERROR WAS DETECTED, OR (2) SEQUENCER PROCESSED THROUGH DATA SECTOR Y. DETECTED ERRORS ARE REPORTED TO THE DRIVE INTERFACE STATUS REGISTER 510.
771
IS BIR BIT 408 SET?
NO
YES
772
WERE ANY ERRORS REPORTED TO THE DRIVE INTERFACE STATUS REGISTER 510?
YES
NO
773
DOES BDSEC REGISTER 584 INDICATE THAT ALL N DATA SECTORS WERE READ/WRITTEN WITHOUT ERROR?
YES
NO
774
DOES BDSEC REGISTER 584 INDICATE THAT ERROR OCCURRED AFTER THE TARGET DATA SECTOR Y?
YES
NO
775
READ LDSEC REGISTER 583 TO FIND THE EXACT DATA SECTOR DURING WHICH THE ERROR OCCURRED AND GET ERROR STATUSES OUT OF DRIVE INTERFACE STATUS REGISTER 510 FOR ERROR HANDLING PROCESSING.
776
RETURN TO STEP 760.

FIG. 64B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/17544

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G11B 5/012
US CL :360/98.01
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 360/98.01, 99.06, 99.02; 369/75.1, 75.2

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X/Y	JP 60-80162 A (UEHARA) 08 May 1985, abstract and figures 4-9.	(1-2 and 4-6)/(3, 7-8 and 9-11)
Y	US 5,233,490 A (NAKANISHI) 03 August 1993, figure 1.	3
Y	US 5,243,480 A (TANGI et al) 07 September 1993, figures 1-3.	7-11
A	US 5,249,091 A (SHIMIZU et al) 28 September 1993, figure 1.	1-11
A	JP 60-79556 A (MORIMOTO) 05 July 1985, figures 2 and 3.	1-11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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